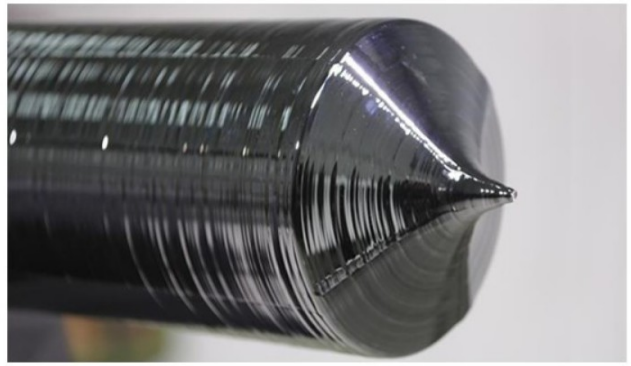
Power Electronics: From Semiconductor Basics to Advanced Design and Testing: part 2

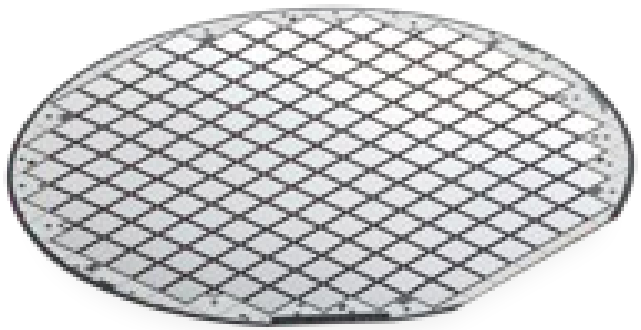
Matteo Santoro, Commissione Elettronica e Microelettronica Ordine degli Ingegneri della provincia di Roma

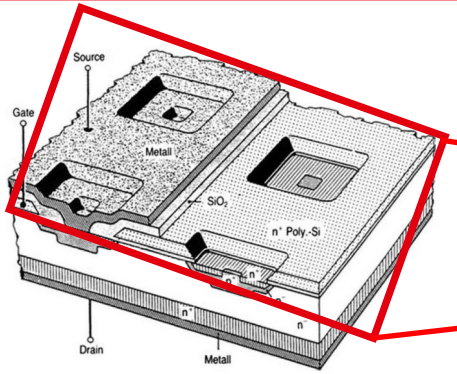
Product Manager Semikron Danfoss.

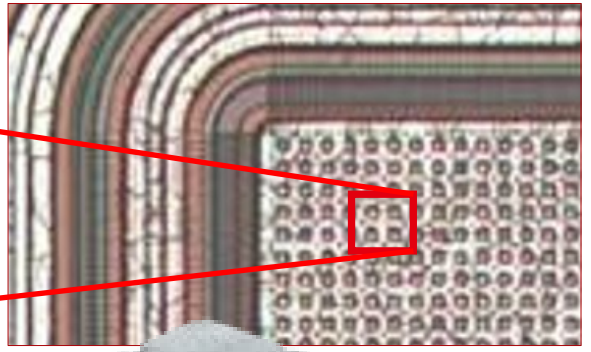
Ordine degli Ingegneri della Provincia di Roma

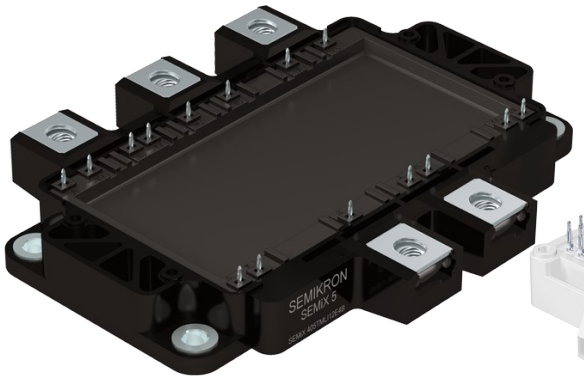
SEPTEMBER 26

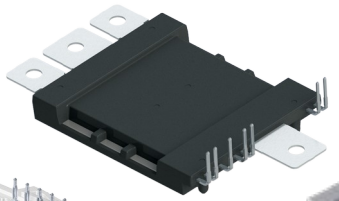


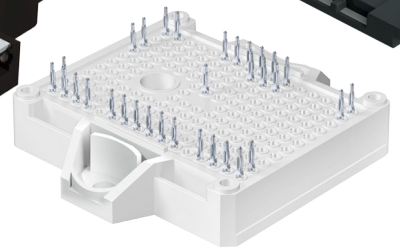










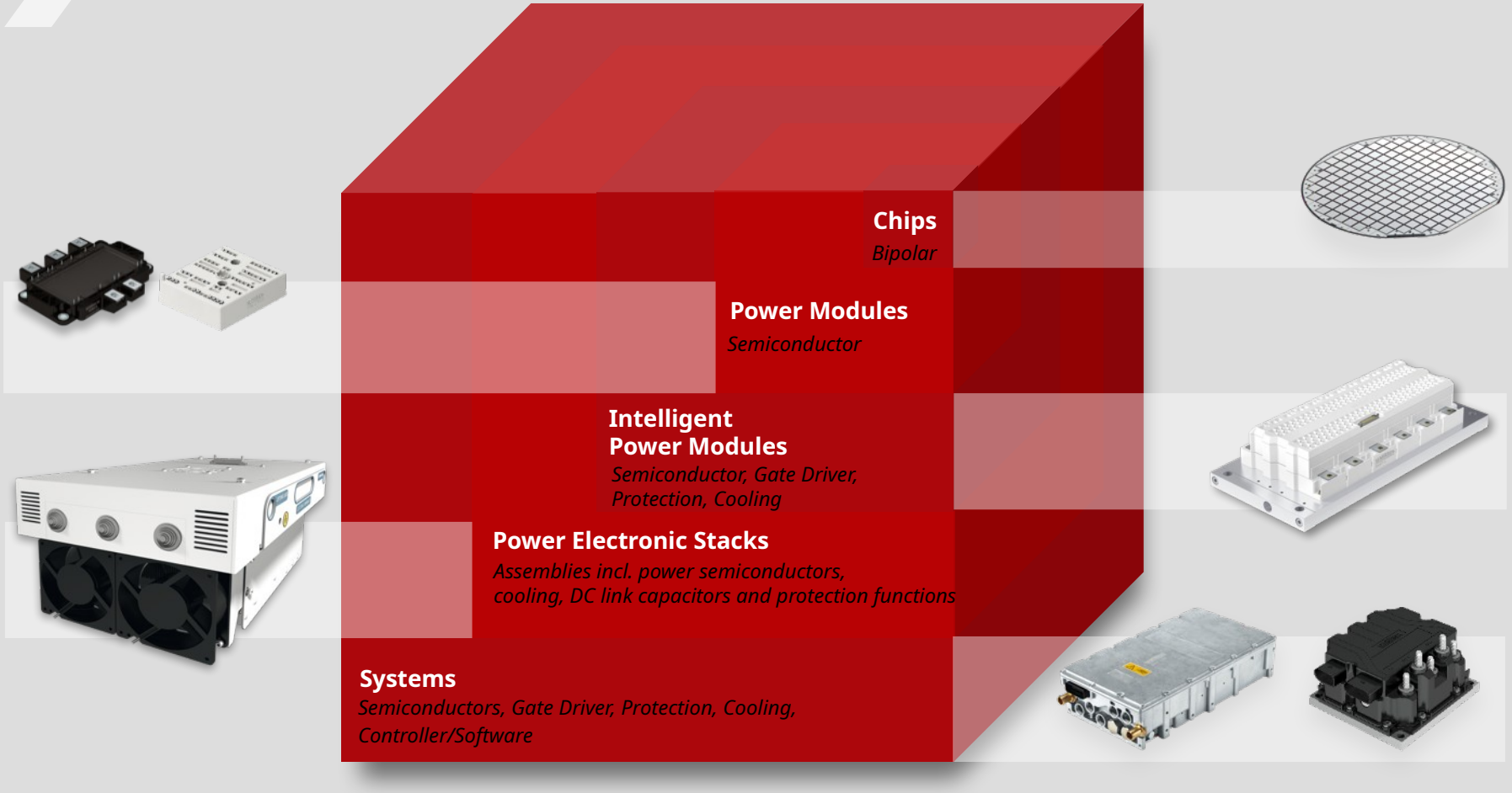


Power Electronics

4. Power Module Design and Manufacturing

From Chip to System

Value Added Levels



Manufacturing substrate : «Power Hibrid»

Thermal capacity for different material's substrate

- $Al_2O_3 : 24\frac{W}{m \cdot K}$,(Allumina)
- AlN da 130 a $180\frac{W}{m \cdot K}$ (Alluminio Nitruro).

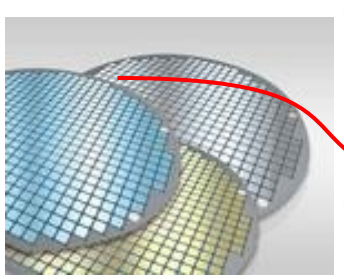
Thermal expansion coefficient is comparable with silicon

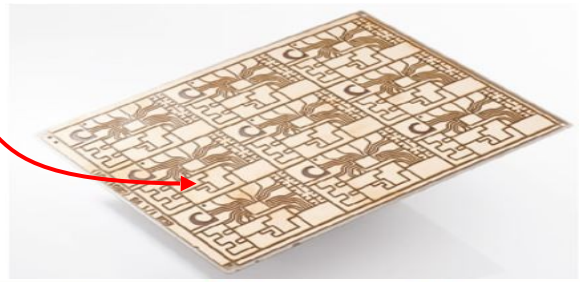
Al_2O_3 è di $7.1\frac{ppm}{K}$

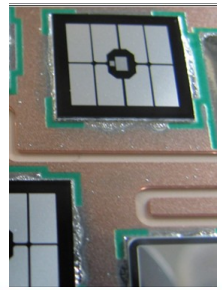
AlN è $(4.1\frac{ppm}{K})$

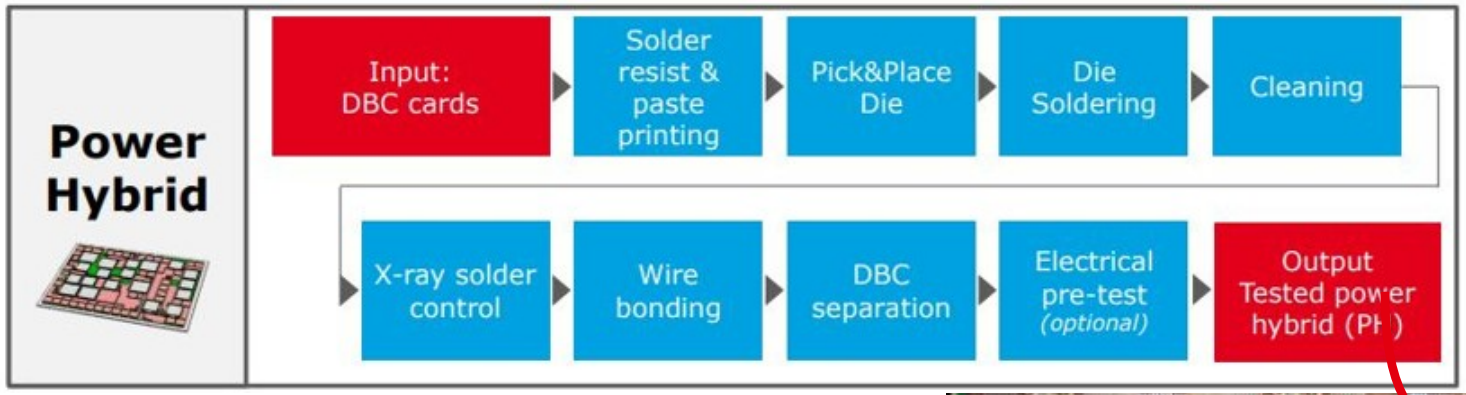
silicio $(\ 4.0\frac{ppm}{K})$

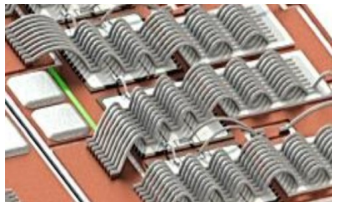
DCB: Direct Copper Bonded (pre-lasered or laser-cut in the manufacturing line)

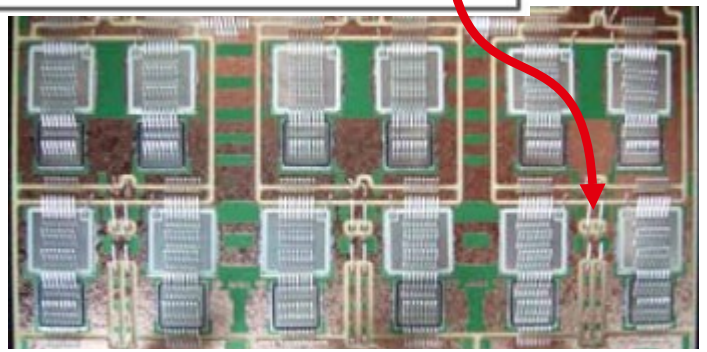




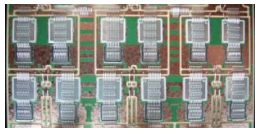




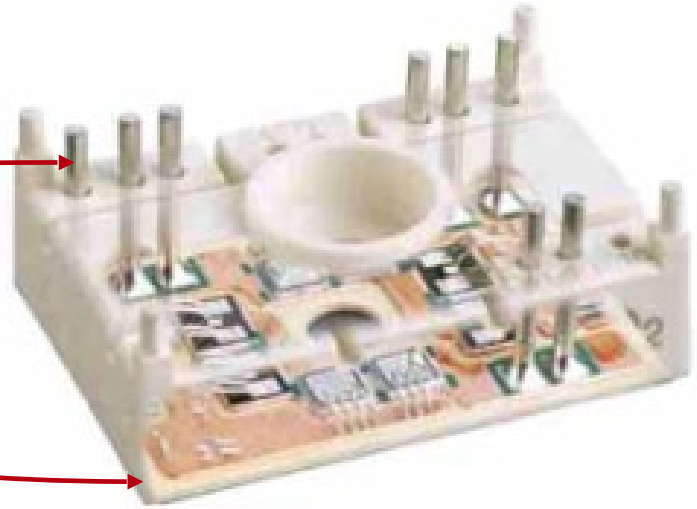




Module Manufacturing (dal Power Hibrid) (DA3, DB3…)

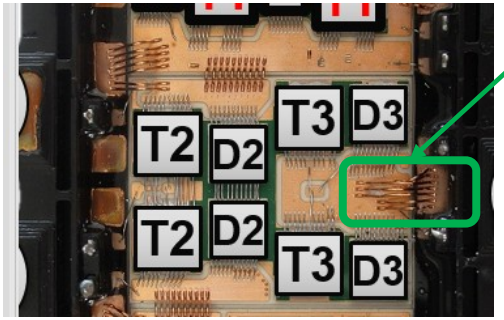


Power hybrid (PH) → Pins (P&P + soldering) → Housing, gluing and UV curing → Soft molding, vacuum and Thermal curing → 100% final measurement → Laser marking → Output Finished Module



- Test static Elettrici
- Test dinamici (doppio impulso
- Test di isolamento (2500 VAC e.g.)
- Test visive

- Rilavorazione?



2nd wire bonding optional (copper)

Resa (Yield) =(1/scarto)

= N. totale moduli buoni /Numero totale scarti

Power Modules Classification

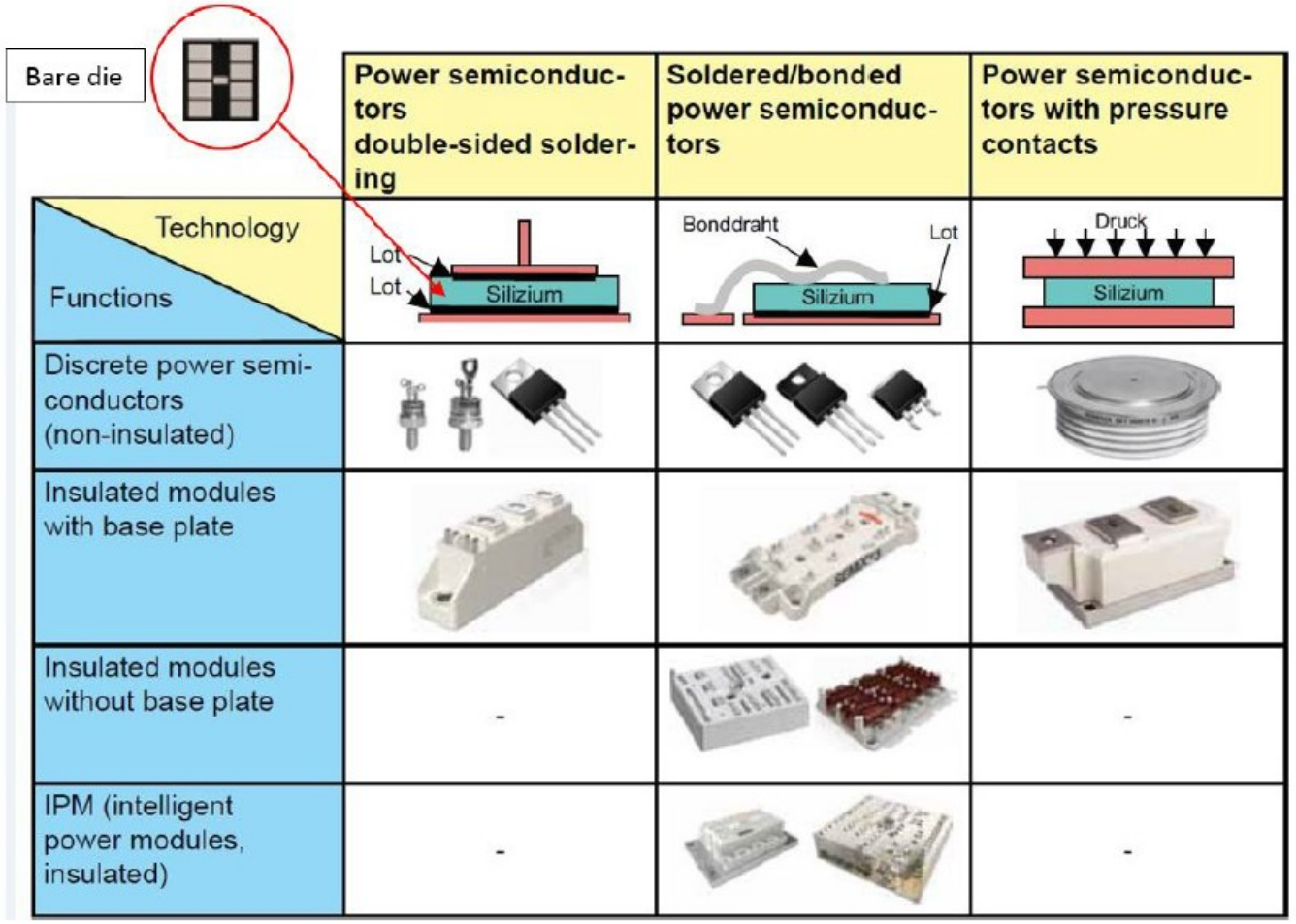
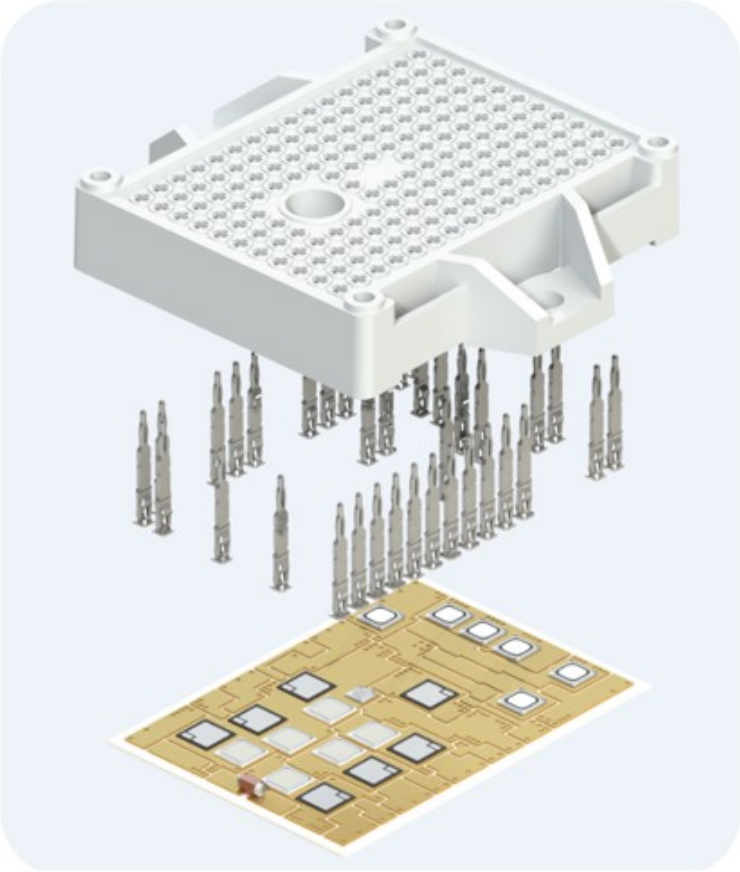
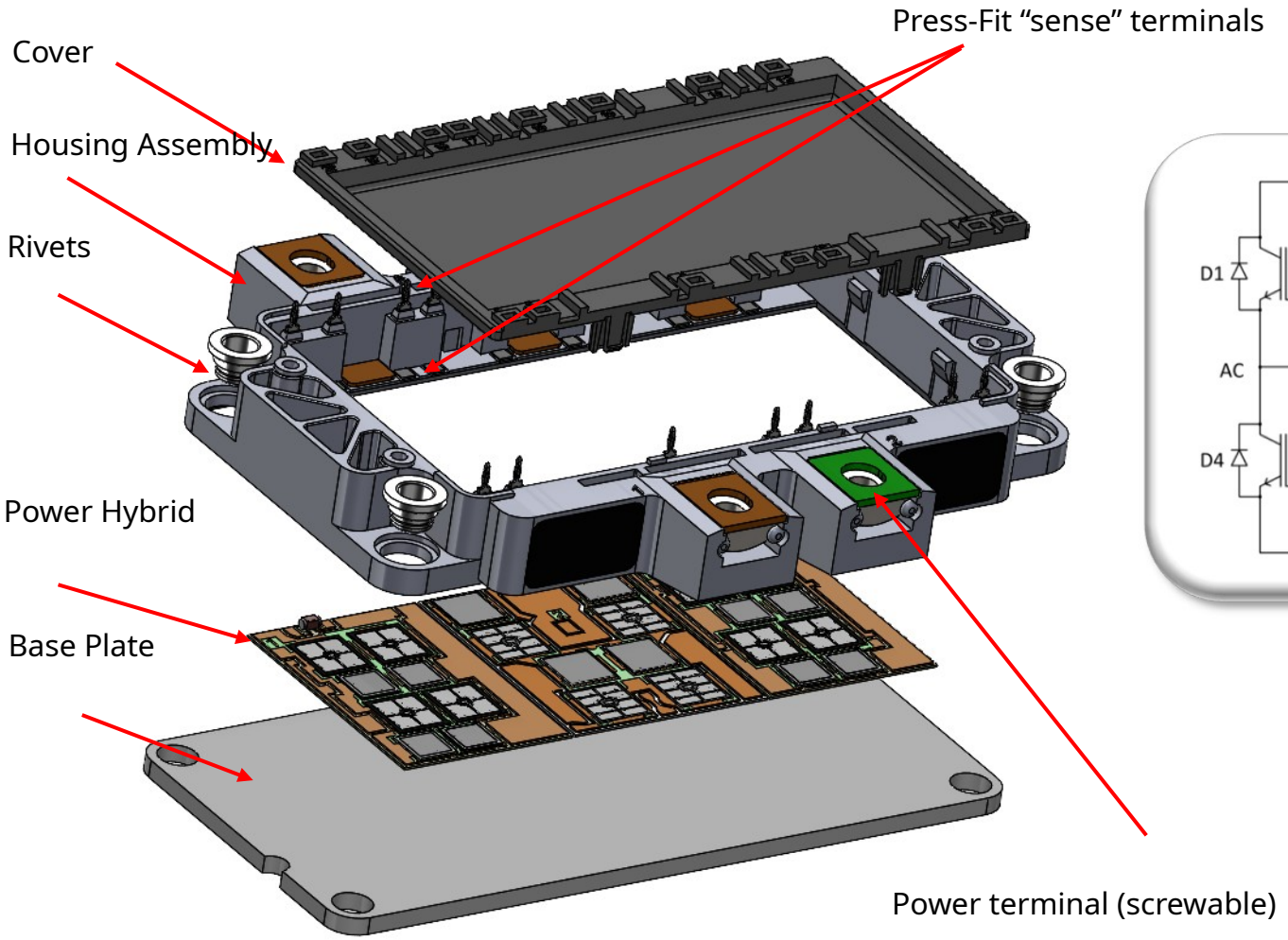
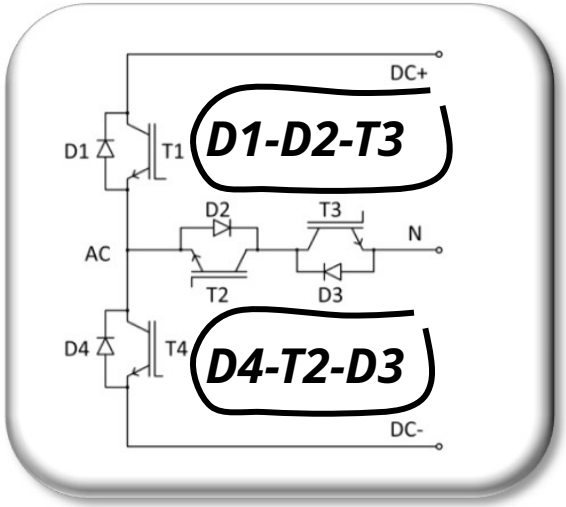


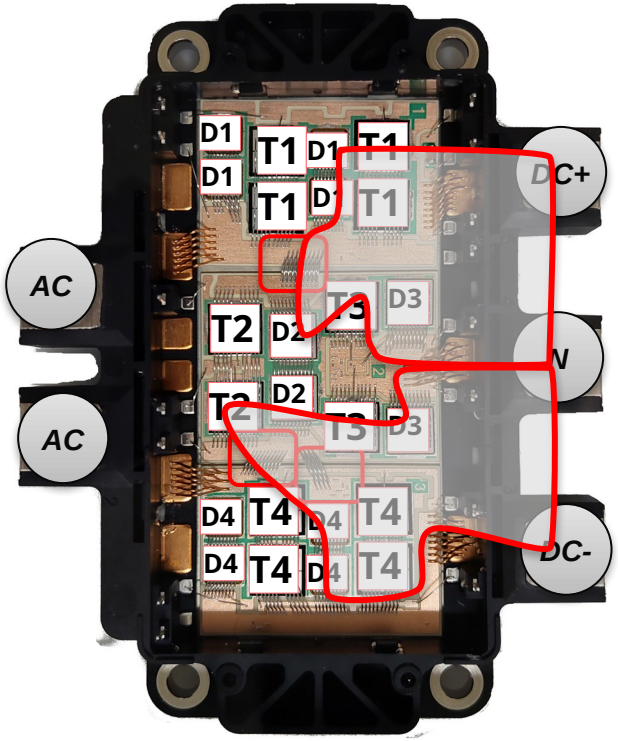
Figura 1.4: Classificazione dei moduli di potenza in funzione della tecnologia



Example: Power Module with base-plate





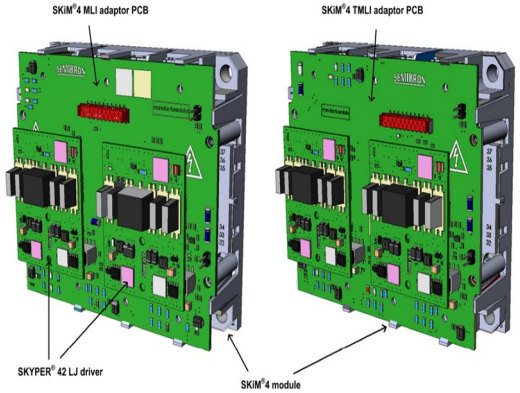


SKD “true” 400A TNPC

(SEMiX405TMLI12E4B)

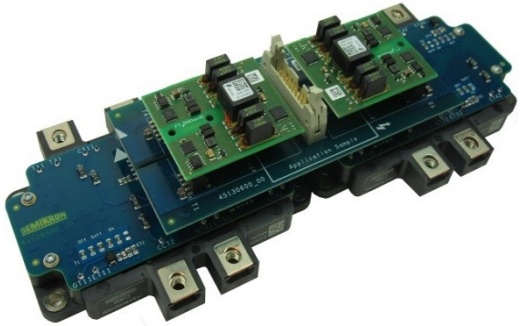
… Driver…

SKiiM-4&5

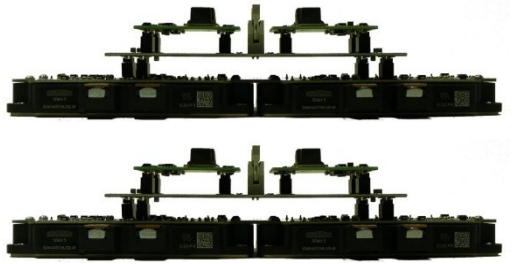


SEMIX-5

100/125 KW Solar



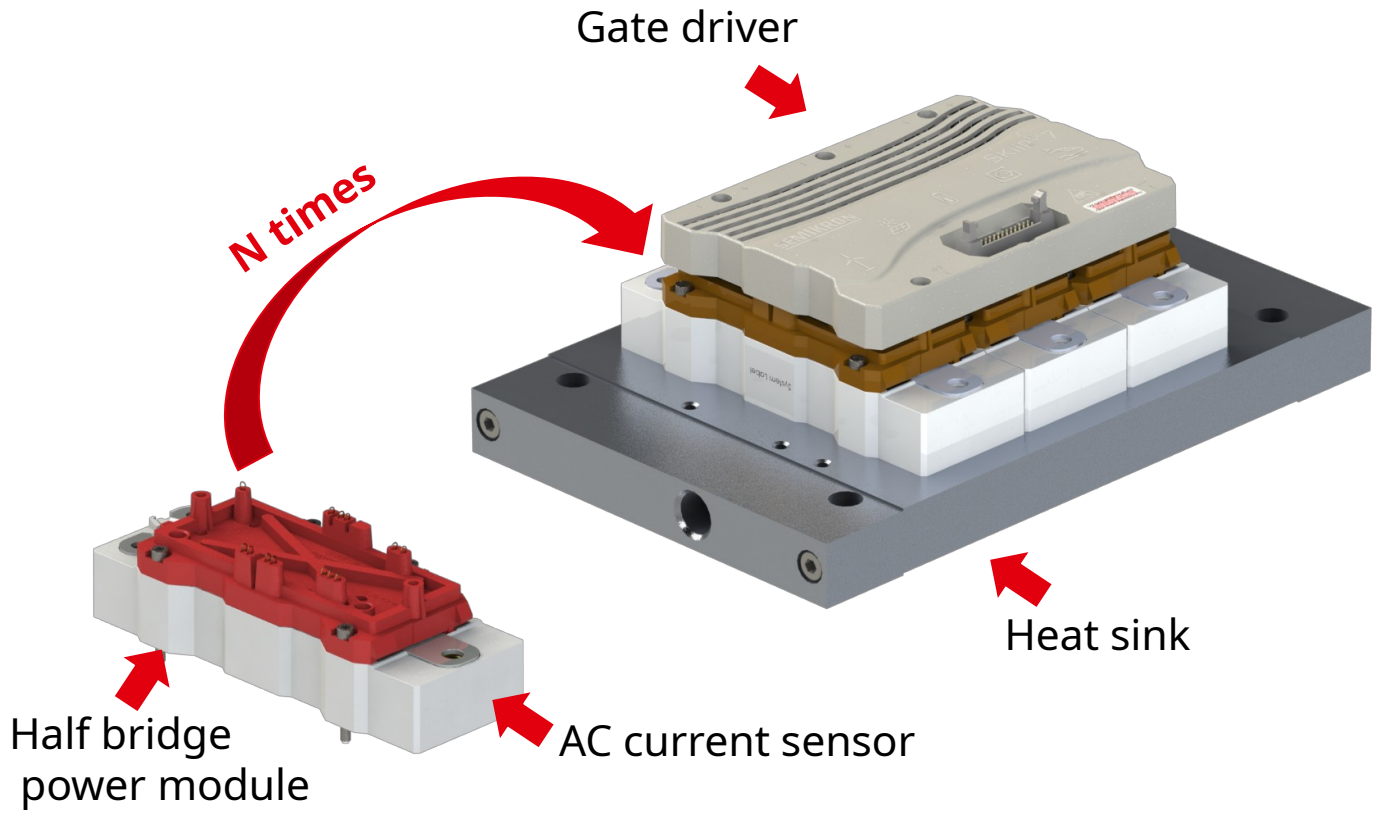
250 KW Solar



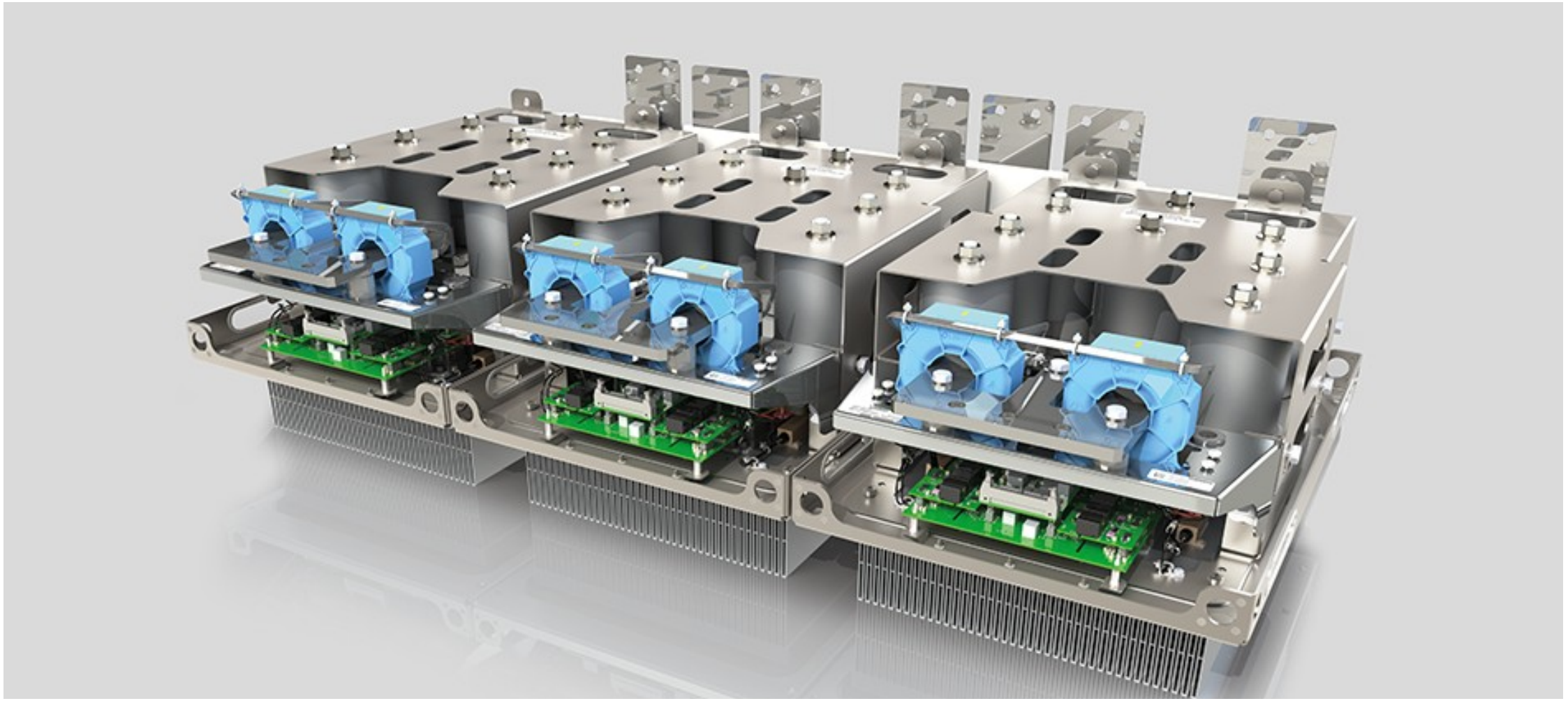
500 KW Solar

...Intelligent Power Module ...

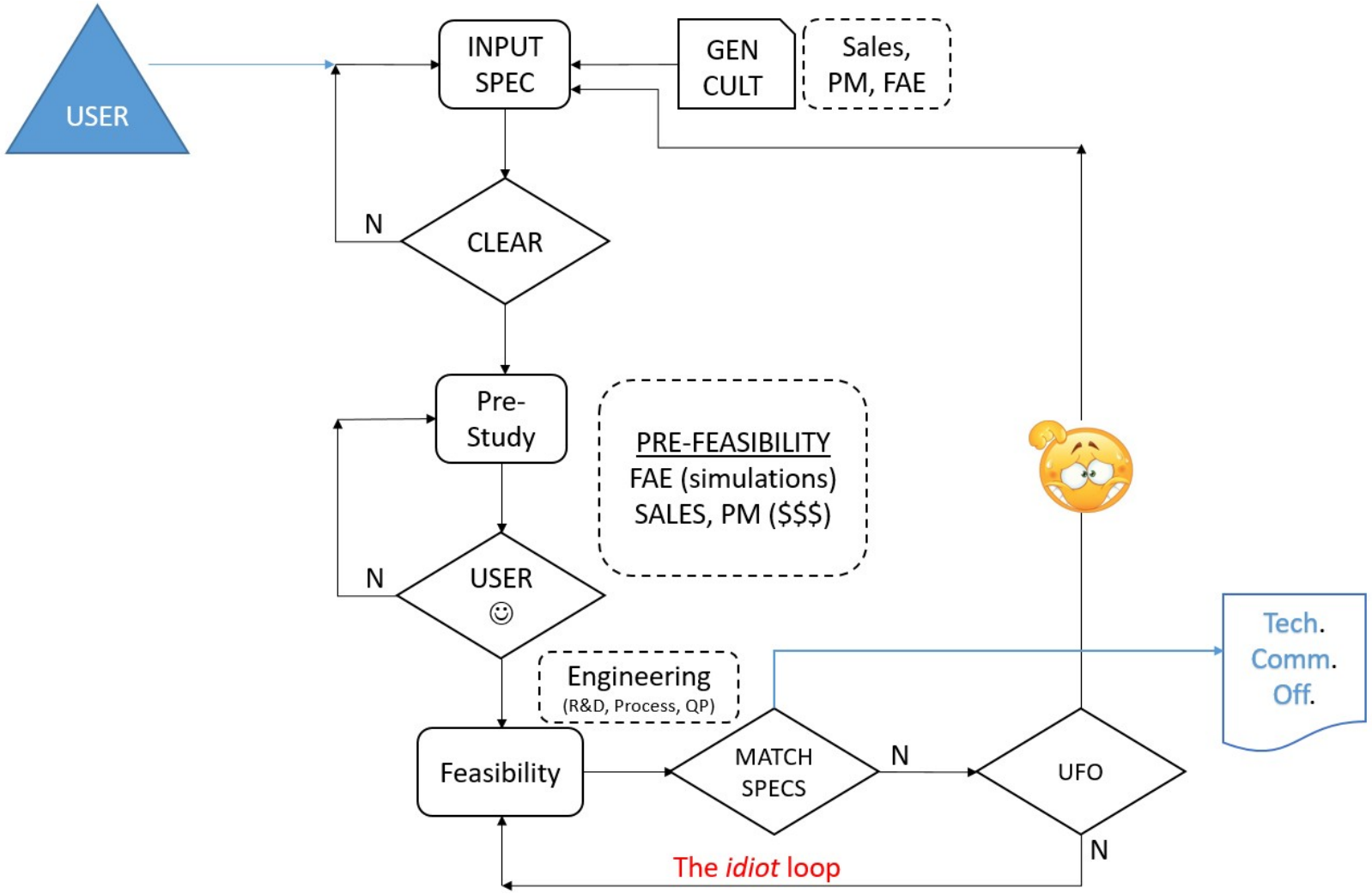
- Intelligent power module with integrated driver, sensors and cooler
- High power halfbridge or sixpack configuration (0.5-2MW)
- Blocking voltage 1200V or 1700V
- Current ratings 500-3600A
- Safety isolated current, temperature and voltage sensors
- Basic protection functions



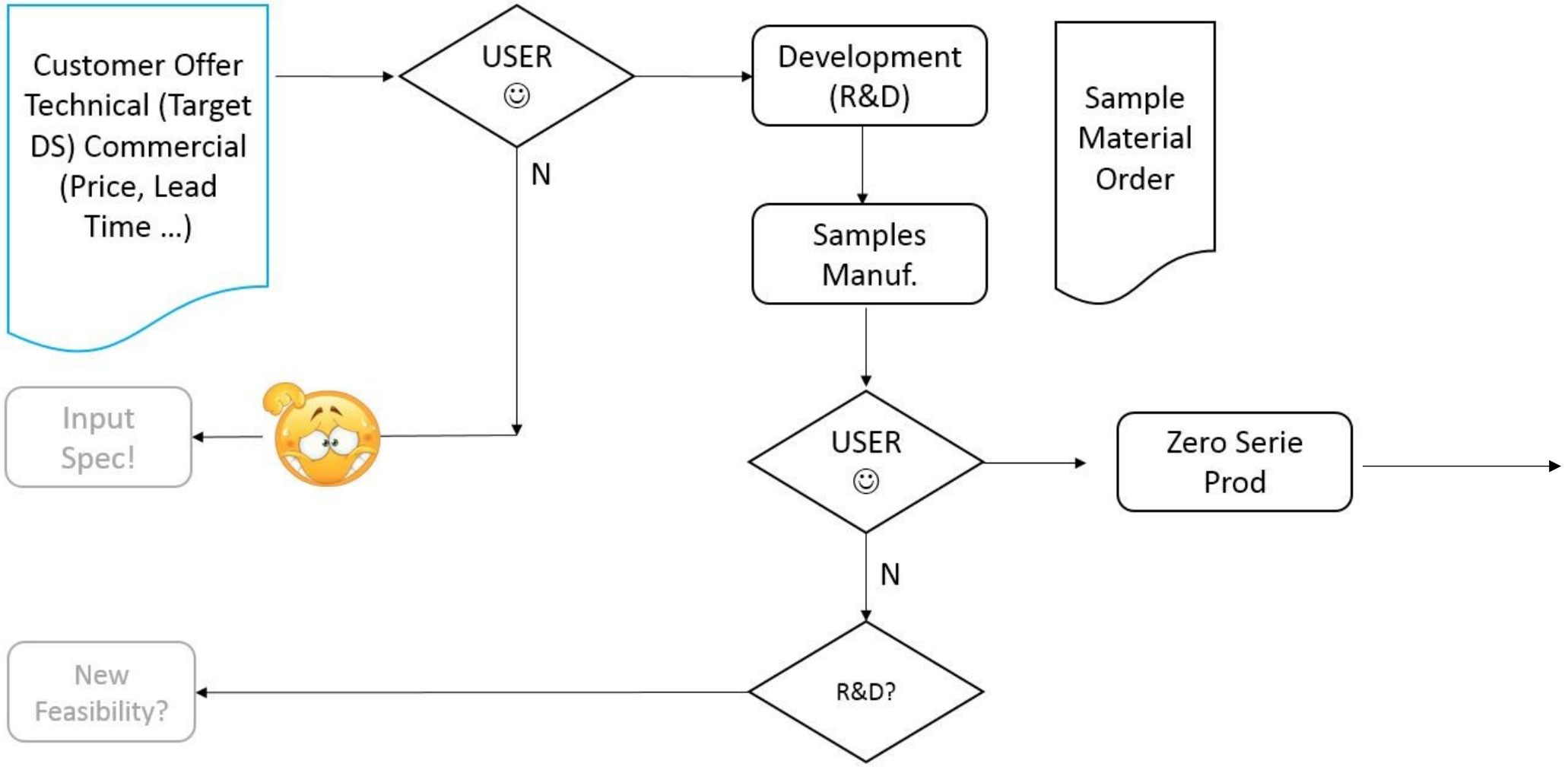
… Stack



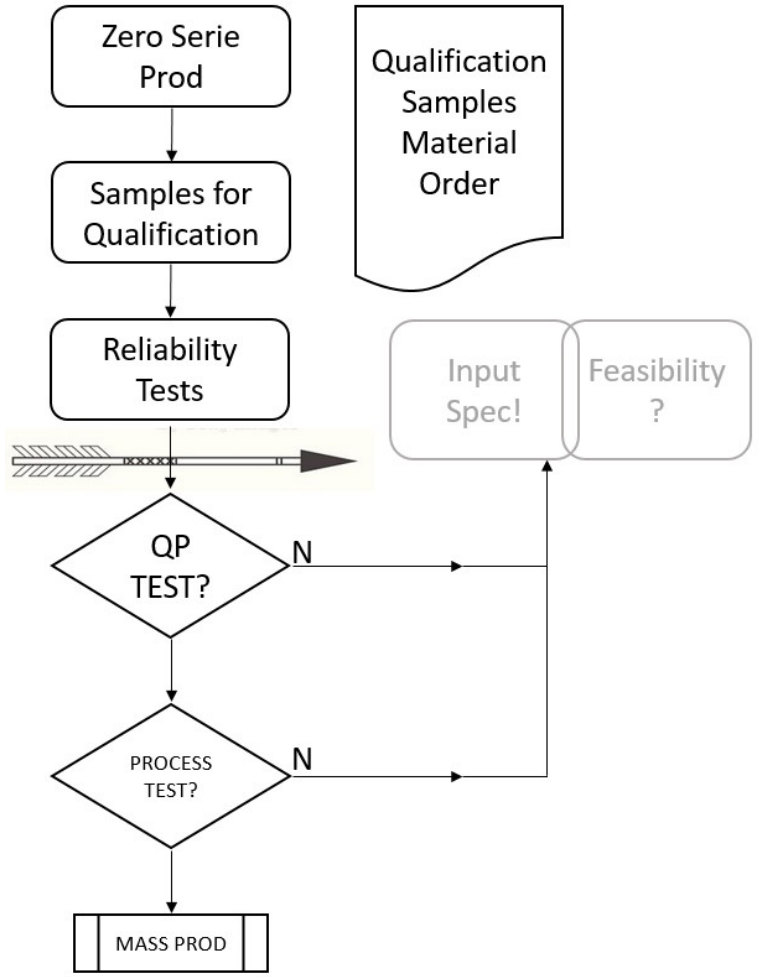
Design Flow 1/3



Design Flow 2/3



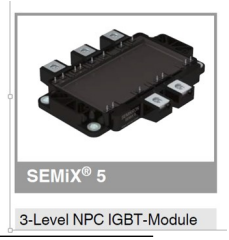
Design Flow 3/3



Power Electronics

5. Datasheet

Datasheet, Absolute Maximum Ratings



- V_{CES} (**Max BLOCKING Voltage**!)

GE shorted! This is Max value which should be

IGBT turned off

For Diode is V_{RRM}

$$V_{cc} + L_\sigma \frac{di_{OFF}}{dt} < V_{CES}$$

depend on switching speed!!!

- I_C. **max conduction current** strongly dependent by Rth!

$$I_C = P_{totMAX} / V_{CE(sat)} = \frac{T_{j(max)} - T_C}{R_{th(j-c)}}$$

RBSOA

- I_{CRM} (*) Repet. Pulse Curr.
- V_{GES} (max GE sustainable voltage)
- t_{psc} (*10us for IGBT4, NOT possibile M7!)*
- T_j ($T_{v,jmax}$ $T_{j,op}$)

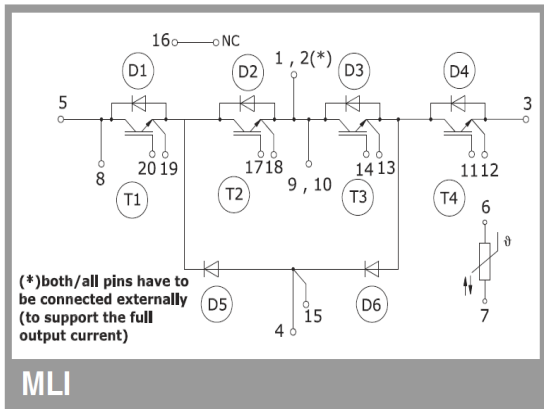
(*)

I_{CRM}	$I_{CRM} = 3 \times I_{Cnom}$	(IGBT4)
I_{FRM}	t_p = 100µs; repetition rate limited by T_{jmax}; Duration: <10% of total time	SiC D

SEMiX305MLI12E

SEMiX® 5

3-Level NPC IGBT-Module



MLI

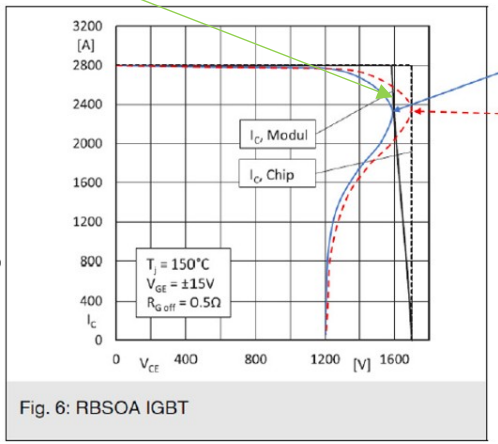
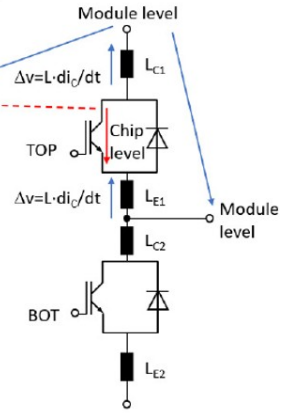
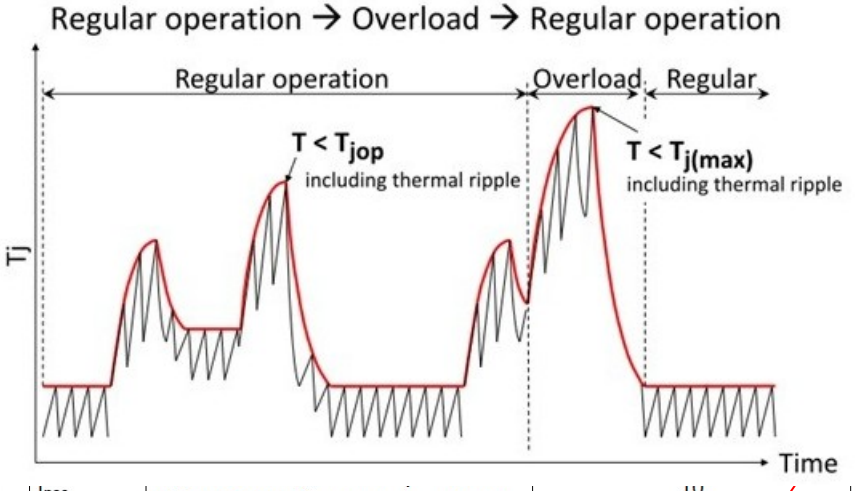


Fig. 6: RBSOA IGBT





t_{psc}	V_{CES} ≤1200 V	10	µs
T_j		-40 ... 175	°C

IGBT2

- Product reliability results valid for T_j ≤150°C (recommended Tj,op= -40…+150°C)

V
A
A
A
A
V

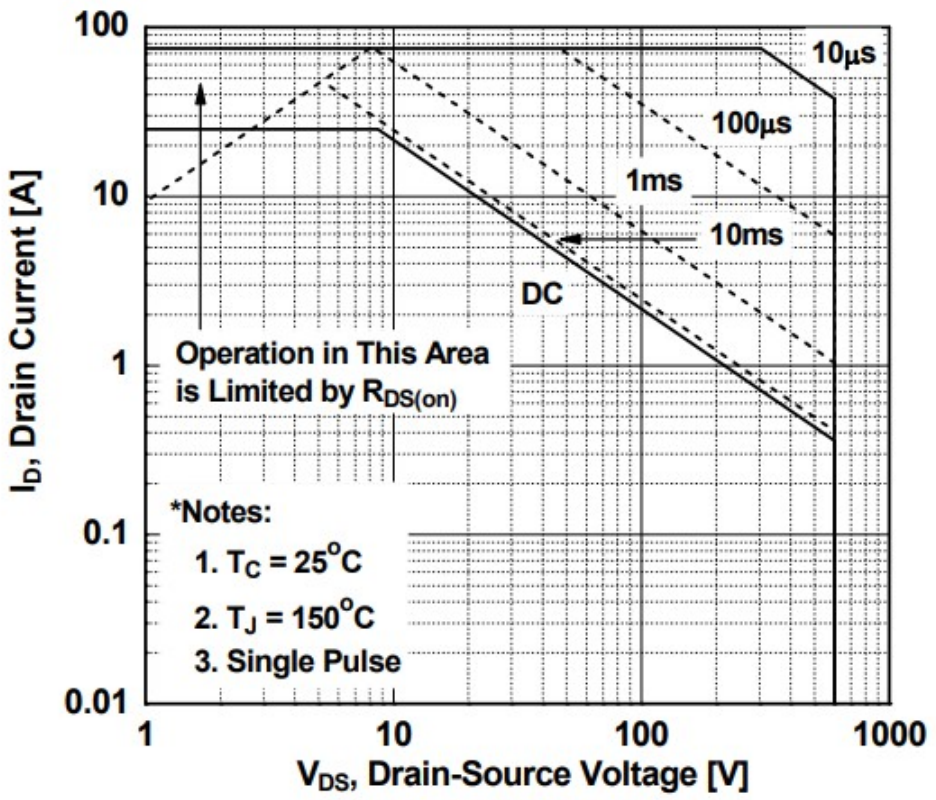
The maximum allowable temperature for the chip during conventional continuous operation is specified in $T_{j(op)}$. Please ensure the maximum chip temperature stays at or under $T_{j(op)}$ during conventional continuous operation. The maximum allowable temperature for a chip during short-term overload or abnormal operation is specified in $T_{j(max)}$.

"SHOULD BE" always present but is a MUST for "small chips" like SiC where bond wires are limited, in this case IFRM is less then 3 times ICnom!

SOA (for Linear Amplifier! Not used in Switcing Power Elec.)

- SOA is different is FORWARD current and maximum nominal current
- Not available in modern datasheet
- Depend on the time and limited by Ron
- SOA is mainly used or “linear operation” in CONTINUE operation which is typical of transistor in Active Area (so this is the reason you do not find often in Power Module working in PWM)

Figure 9. Maximum Safe Operating Area



FAIRCHILD SEMICONDUCTOR®

FCH25N60N

N-Channel MOSFET

600V, 25A, 0.126Ω

Features

- $R_{DS(on)}$ = 0.108Ω (Typ.) at V_{GS} = 10V, I_D = 12.5A

- Rof FCH25N60N N-channel Mosfet

Datasheet, STATIC Characteristics

3-Level NPC IGBT-Module

- $V_{CE(sat)}$ (ON
  - Chip level Effect of $R_{CC'-EE'}$
- $V_{GE(th)}$
- V_{CE0}, r_{CE} (values at ON state) VCEtot is provided by the linear model of the ON-State Diode , see after)

$$V_{CE(sat)} = V_{CE0} + r_{CE} \cdot I_C$$

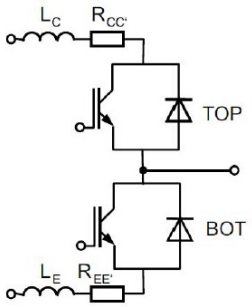
diode model ON

- I_{CES} (max leakage in blocking state, limit for reliability test: It defines ithe value the module should withstand **AT THE END of 1000hours HTRB** (see reliability); it is ***PRODUCTION PROCESS*** *dependent!*: and COULD BE different with respect **I_{CES} value defined at bare dies level! (very often is different)**
- C_{ies}, C_{oes}, C_{res} (directly linked to bare die characteristics)

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
IGBT1						
$V_{CE(sat)}$	I_C = 300 A V_{GE} = 15 V chiplevel	T_j = 25 °C		1.80	2.05	V
		T_j = 150 °C		2.20	2.40	V

Static Characteristics (tested on wafer), T_{vj}=25°C BARE DIE IGC142T8RM

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=5.7mA	1200	-	-	
Collector-emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=45A	0.97	1.15	1.32	V



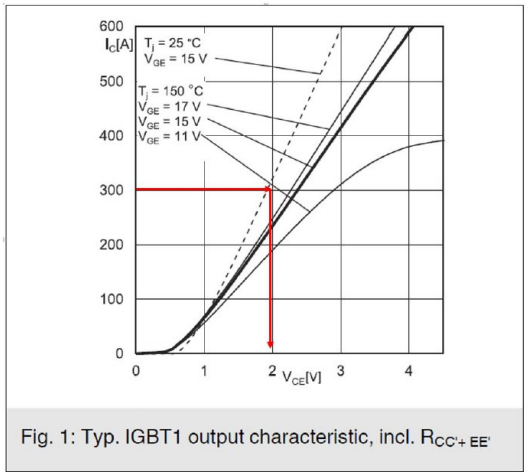
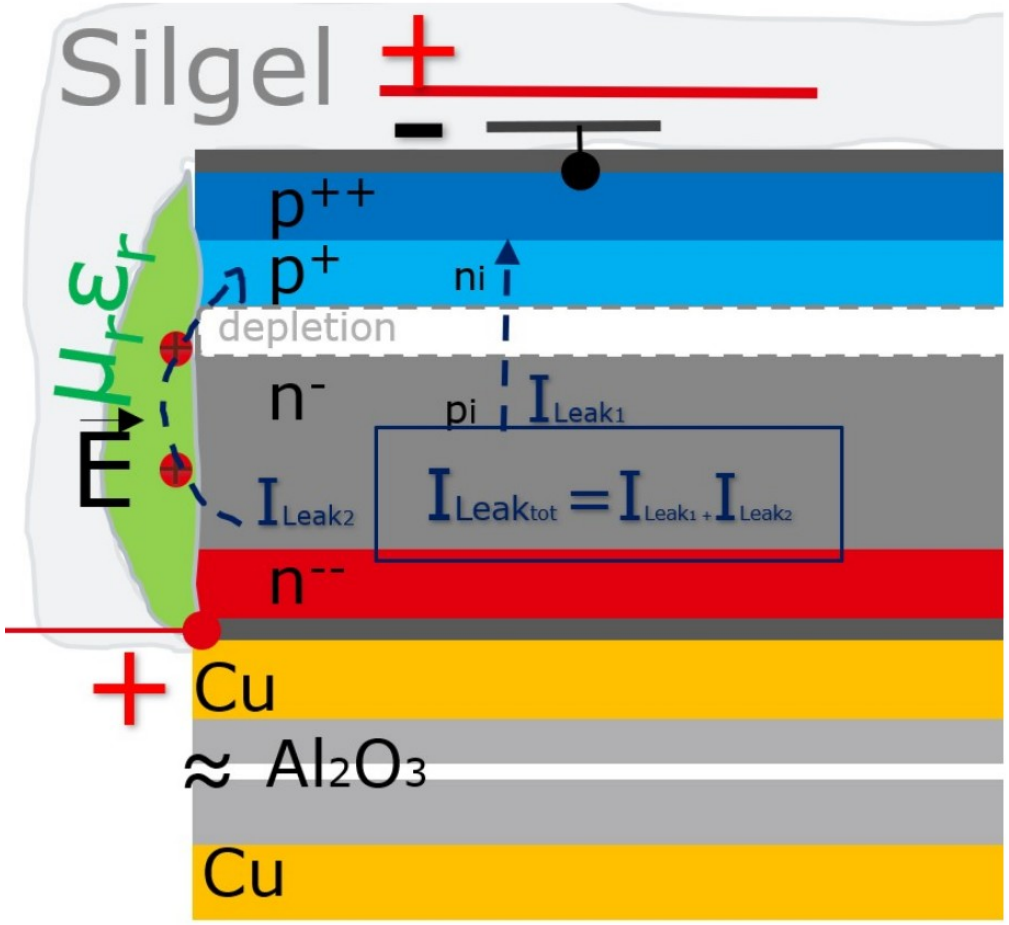


Fig. 1: Typ. IGBT1 output characteristic, incl. $R_{CC'+EE'}$

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
IGBT1						
$V_{CE(sat)}$	I_C = 300 A V_{GE} = 15 V chiplevel	T_j = 25 °C		1.80	2.05	V
		T_j = 150 °C		2.20	2.40	V
V_{CE0}	chiplevel	T_j = 25 °C		0.80	0.90	V
		T_j = 150 °C		0.70	0.80	V
r_{CE}	V_{GE} = 15 V chiplevel	T_j = 25 °C		3.3	3.8	mΩ
		T_j = 150 °C		5.0	5.3	mΩ
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 12 mA		5	5.8	6.5	V
I_{CES}	V_{GE} = 0 V, V_{CE} = 1200 V, T_j = 25 °C				4.0	mA
C_{ies}	V_{CE} = 25 V V_{GE} = 0 V	f = 1 MHz		18.6		nF
C_{oes}		f = 1 MHz		1.16		nF
C_{res}		f = 1 MHz		1.02		nF
Q_G	V_{GE} = -8V...+15V			1700		nC
R_{Gint}	T_j = 25 °C			2.5		Ω

Still some consideration on I_{CES} and how is defined in Datasheets

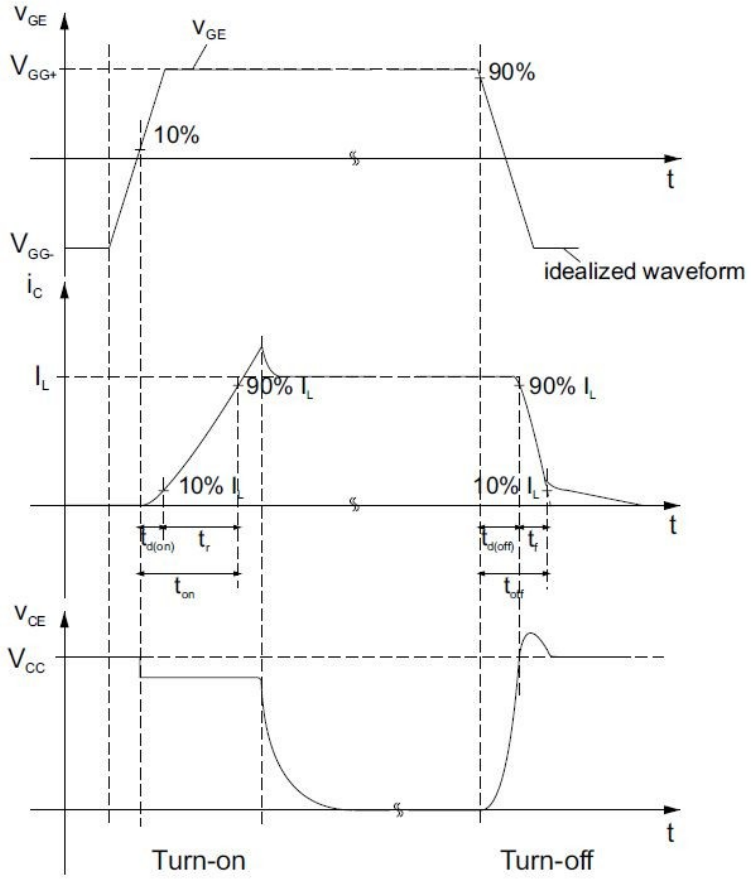
- Even in *n*-type are presents p_i (and in *p*-types n_i) which are intrinsic in semiconductors
- This cause I_{Leak1} in inverse polarization which is “small” compared to forward current (which is very small as $n_i << p$ and $p_i << n$): some µA in IGBT4 for instance.
- I_{leak}=Func(technology, geometry, if several chips in antiparallel, process soldering, reliability tests…)
- Process assembly → introduction of dielectric impurity on the p-n “naked” vertical junction → surface ione impurity further I_{Leak2} contributor → $I_{LeakTot=} I_{Leak1}+I_{Leak1} > I_{Leak1}$
- No clean improve. Synther ok (but Ag+!)
- Reliability → 1000H HV3TRB further impurity (H2O iones, dendrides, electromigration) → I_{Leak3}



I_{CES} defined in IGBT **MODULE** datasheet usually is higher than ICES in bare die datasheet. And is also linked to TEST SPECIFICATION

Warning: Test specification define also the production scrap rate!

Datasheet, Characteristics (switching : Eon, Eoff, rise time, fall time)



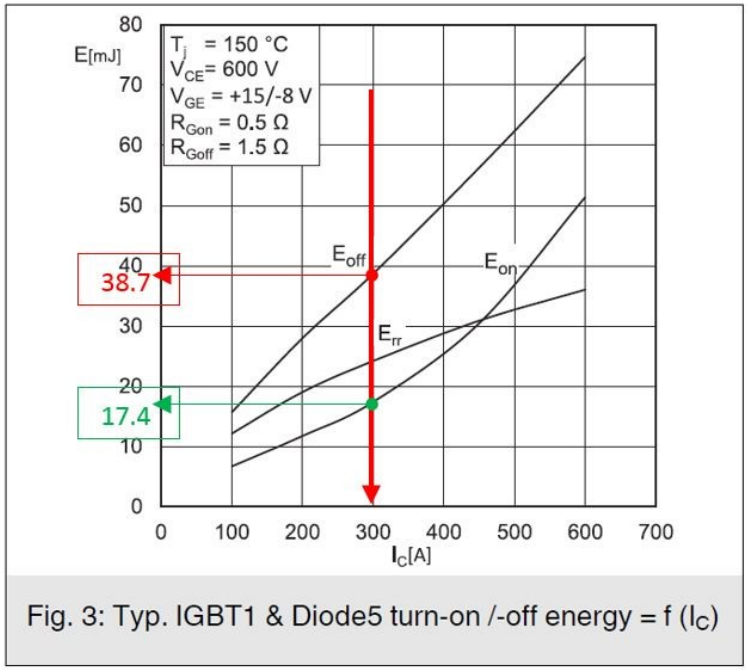


Fig. 3: Typ. IGBT1 & Diode5 turn-on /-off energy = f (I_C)

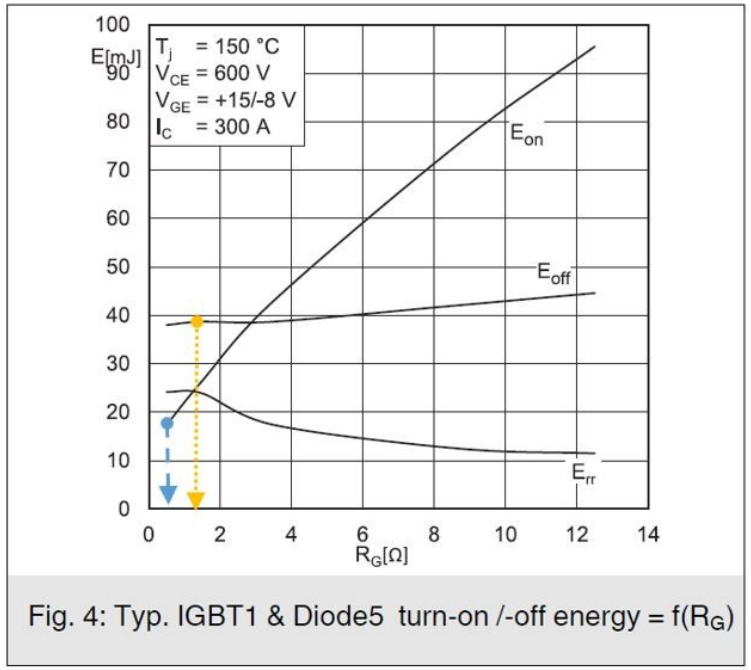
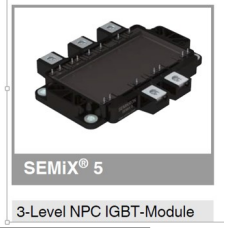


Fig. 4: Typ. IGBT1 & Diode5 turn-on /-off energy = f(R_G)

E_{on}	V_{GE} = +15/-8 V $R_{G\,on}$ = 0.5 Ω	T_j = 150 °C	17.4	mJ
$t_{d(off)}$	$R_{G\,off}$ = 1.5 Ω	T_j = 150 °C	488	ns
t_f	di/dt_{on} = 5700 A/µs	T_j = 150 °C	148	ns
E_{off}	di/dt_{off} = 2300 A/µs dv/dt = 3500 V/µs	T_j = 150 °C	38.7	mJ

Datasheet, Characteristics: commutation speed



C_{ge} in and out with CE shorted

C_{ge} with CE direct

- di/dt$_{OFF}$

chip transcond.

$$\frac{di_{Coff}}{dt} = g_{fs}\frac{V_{GE}}{C_{IES}\cdot R_{GOFF}}$$

- Overvoltage during switch off

$$dV = L\cdot\frac{di_{OFF}}{dt}$$

Note:

L = F[Area_Module + Area_driver]

di/dt$_{OFF}$ = F[g,C,Rgoff]

di/dt$_{OFF}$ QP dynamic bench >> di/dt$_{OFF}$ production DPT (x4!)

L(dyn-bench QP) << L(prod DPT)

→ compensation!

Symbol	Conditions		min.	typ.	max.	Unit
IGBT1						
C_{ies}	V_{CE} = 25 V V_{GE} = 0 V	f = 1 MHz		18.6		nF
C_{oes}		f = 1 MHz		1.16		nF
C_{res}		f = 1 MHz		1.02		nF
Q_G	V_{GE} = -8V...+15V			1700		nC
R_{Gint}	T_j = 25 °C			2.5		Ω
$t_{d(on)}$	V_{CC} = 600 V I_C = 300 A V_{GE} = +15/-8 V $R_{G\,on}$ = 0.5 Ω $R_{G\,off}$ = 1.5 Ω di/dt_{on} = 5700 A/µs di/dt_{off} = 2300 A/µs dv/dt = 3500 V/µs	T_j = 150 °C		71		ns
t_r		T_j = 150 °C		51		ns
E_{on}		T_j = 150 °C		17.4		mJ
$t_{d(off)}$		T_j = 150 °C		488		ns
t_f		T_j = 150 °C		148		ns
E_{off}		T_j = 150 °C		38.7		mJ

slower

from QLAB dyn-Bench which is set for max switching speed and min Rg

Important parameters to design gate driver!

Datasheet, Characteristics (Gate Charge, Rth)

Q_G: **Gate charge** *(allows to calculate the average total gate driver current in function of switching f*

$$I_{G(AV)} = Q_G \cdot f_s$$

Gate Driver Design

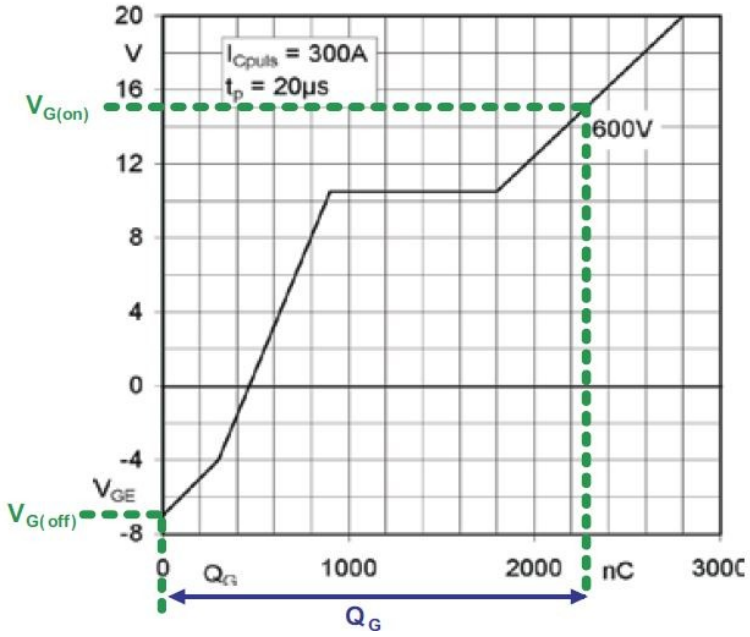
$R_{th(j-c)\ MAX}$: not *very* impacted by TIM (a little bit yes…) , only for modules with baseplate

$R_{th(c-s)}$: strongly dependent by TIM material

Rth measure

- Require thermal stability to be measured
- Thermal interference and statistical impacts

Characteristics					
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
IGBT1					
Q_G	V_{GE} = -8V...+15V		1700		nC
$R_{th(j-c)}$	per IGBT			0.1	K/W
$R_{th(c-s)}$	per IGBT (λgrease=0.81 W/(m*K))		0.077		K/W
$R_{th(c-s)}$	per IGBT, pre-applied phase change material		0.037		K/W



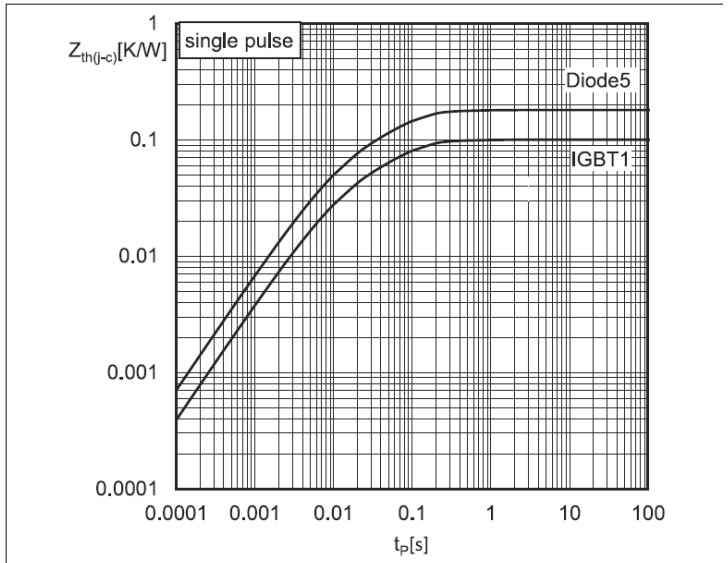


Fig. 9: Transient thermal impedance of IGBT1 & Diode5

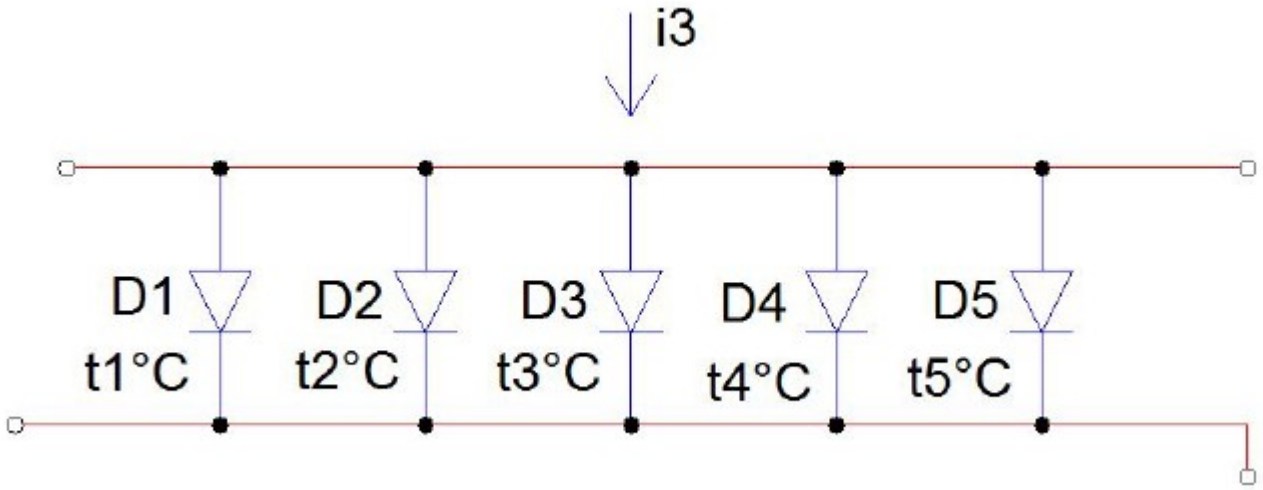
Technological Challenges in Power Electronics Silicon devices manufacturing…

Alternative way to see: As we have seen in slide 64 $n_i(T) \propto T°C$ so intrinsic carrier concentration of silicon increase with temperature → so there is a *decrease* of the resistance of the semiconductor if T increase! (negative coefficient)

All the classic silicon manufacturing challenges

negative temperature coefficient risk to cause thermal runaway in case of chip parallelization!

- The problem of the Thermal runaway and the temperature coefficient troubles of PN junction



V_{ON} function of T

$$V = \frac{KT}{q} ln(I/I_s)$$

- $I_s(T)$

$$I_S(T) = I_S(T_1) \cdot 2^{(T-T_1)/10}[A]$$

I_S **double** every 10°C increase of T°K!

$$\frac{dV_D}{dT} \approx -2.2mV/°C$$

- If V_{On} ↓ then PN voltage barrier is lowering
- Ten current flow easier in the diode→ I increase → T°K increase!

Consideration on the temperature coefficient vs static losses and parallelization: where is evident in the datasheet?

PN junction has negative temperature coefficient

Direct Forward PN Junction

$$V = \frac{KT}{q} ln(I/I_s)$$

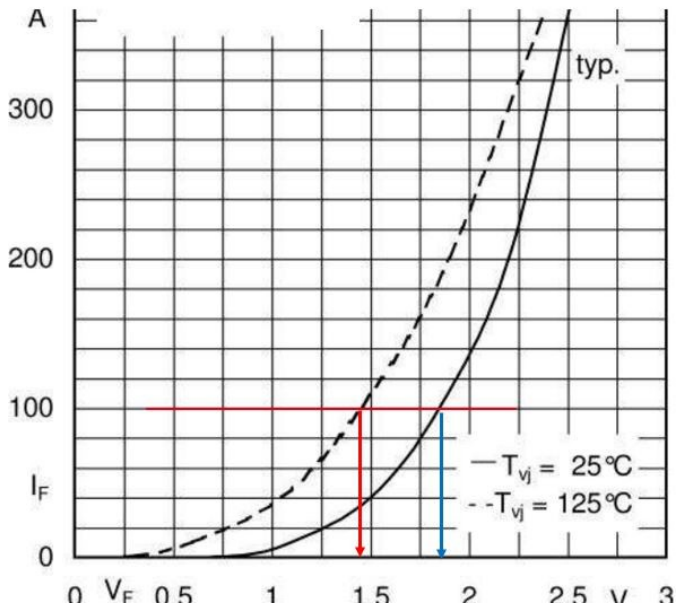
Theoretical analysis of PN junction (Si) indicates that Is change by 7% per °C and because 1.07exp10 ≈ 2 :In other words Is double every +10°C increase. Know Is(T1) Is at T can be calculated with

$$I_S(T) = I_S(T_1) \cdot 2^{(T-T_1)/10}[A]$$

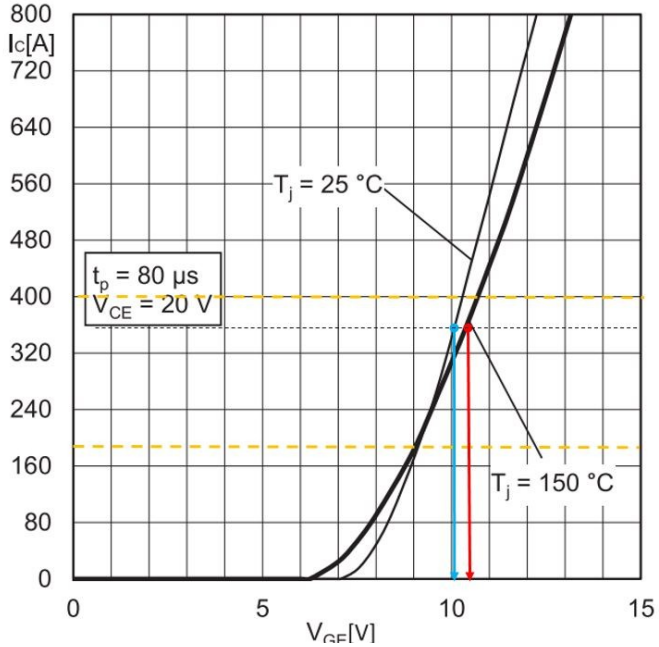
If steady state conditions, increase of temperature cause an increase of Is so Voltage decrease by

$$\frac{dV_D}{dT} \approx -2.2mV/°C$$

In the datasheet the temperature coefficient can be evaluated by analysing the static losses diagram for different temperatures



- Epi diode with negative temperature coefficient
- Good for reducing static losses
- Critical for parallelization



IGBT (or CAL4 diode) and positive temperature coefficient in the nominal range

→ Parallelize is easier!

The design of the intrinsic region (n-), the introduction c implantation, and other techniques can enable power diodes to reverse their temperature coefficient behavio at high currents/voltages from a negative coefficient to positive one.

Turn off Oscillations during reverse recovery in parallel connection of diodes

If a parallel connection is given and oscillations in the reverse recovery of free-wheeling diodes are found, it also has to be investigated whether this is caused by **asymmetrical arrangement of the wirings** and **interconnections.** Oscillations have even been found with a single soft-recovery diode, if the condition is fulfilled that the switching time of the diode t_{rr} agrees **with half the period of the resonance of an LC oscillator circuit.**

In applications with MOSFETs and IGBTs, this can be verified easily: **the modification of the gate-resistor RG of the used IGBT or MOSFET can vary the turn-on slope** of the transistor and with it the commutation velocity di/dt. So the switching time t_{rr} of the diode is modified, and in this case the oscillations should vanish.

for ***SIC MOSFET*** this can be CRITICAL for LAYOUT DESIGN!

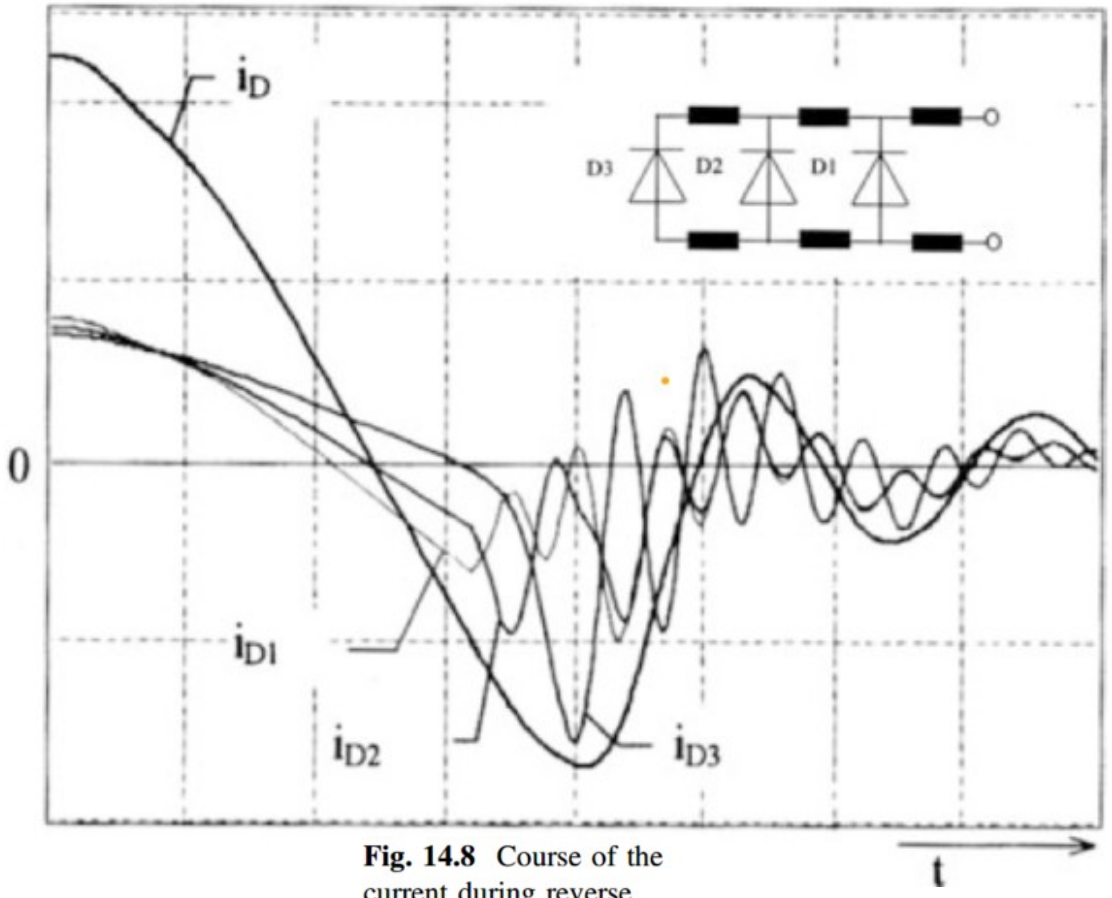


Fig. 14.8 Course of the current during reverse recovery in a parallel connection of diodes with different wiring inductances. 50 ns/div, 50 A/div, 25 °C, V_{bat} approx. 300 V. Figure from [Eld98]

Layout chip positioning – trade off – design choiches

In power modules, often **a lot of single dies are connected in parallel**.
It is very **difficult to give all single dies identical symmetrical conditions** in respect to the length of the current-conducting path to the main terminals as well as in respect to the length of the wiring of the drive signals.

Thermal conditions must be considered, too.

Often trade-offs must be made. Figure 11.33 shows an example of parallel connection of five IGBT dies (to form ONE switch with 1 APD FW Diode), in which asymmetric tracks for the main current to the respective die are given.

The wires for the drive signals, for which also a symmetrical setup is of importance, are not drawn in the schematic circuit diagram of 11.33b.

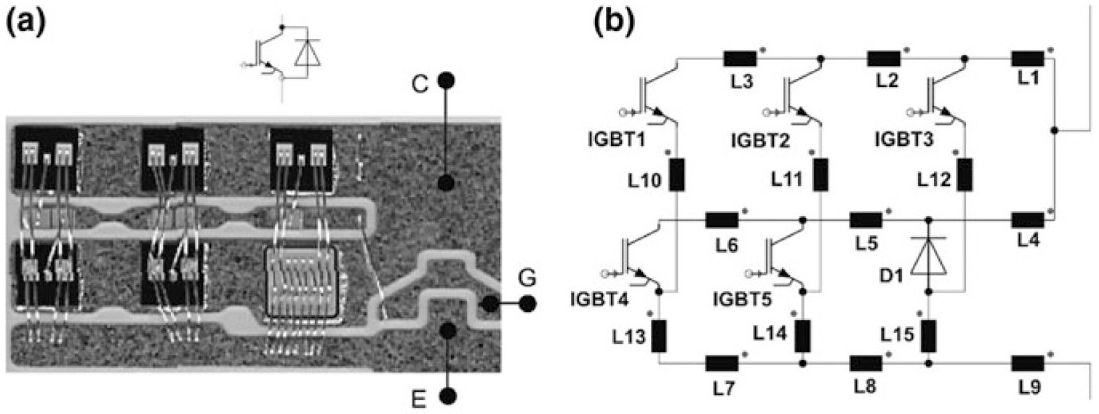


Fig. 11.33 (**a**) Realistic power circuit consisting of 5 parallel IGBT chips and one anti-parallel freewheeling diode chip (**b**) schematic circuit diagram showing the power devices plus the parasitic inductances formed by the current tracks

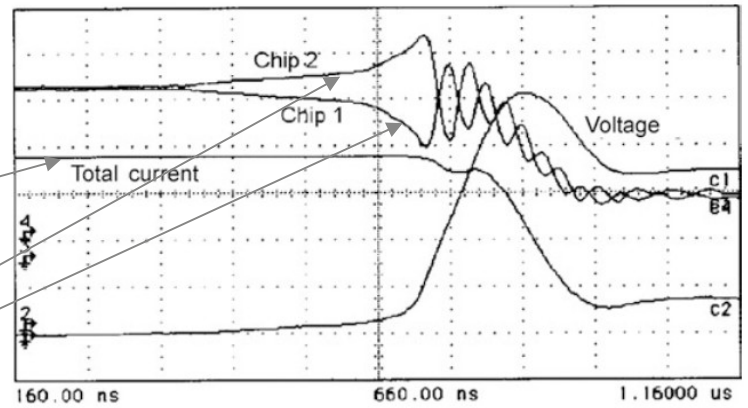


Fig. 14.3 Oscillations of the current in two IGBTs connected in parallel. Gate resistors 6.02 Ω for chip 1 and 6.45 Ω for chip 2. Current 10 A/div, voltage 50 V/div. Figure according to [Pal99] © 1999 EPE

Despite total current appears ok single chips can have

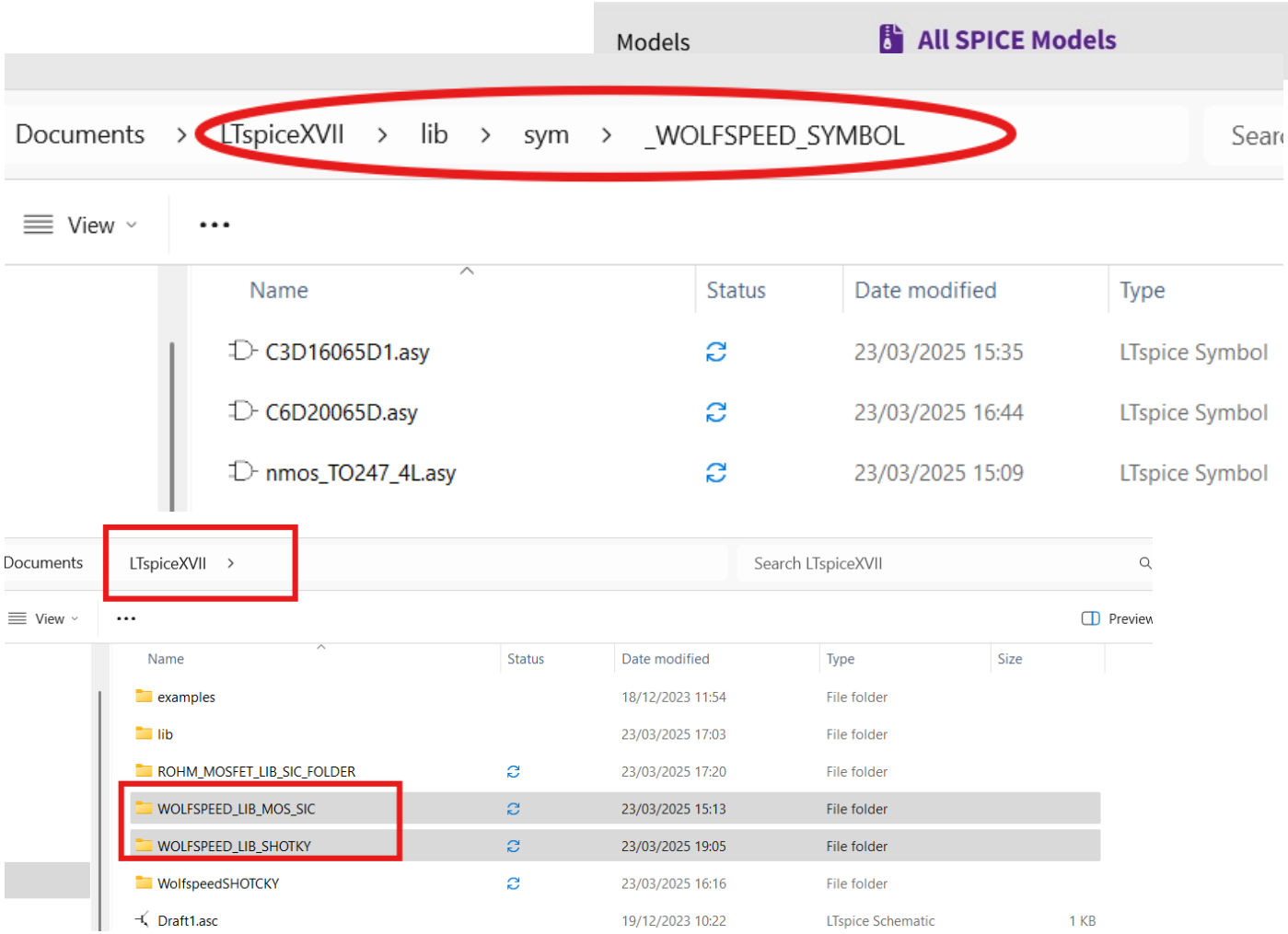
Power Electronics

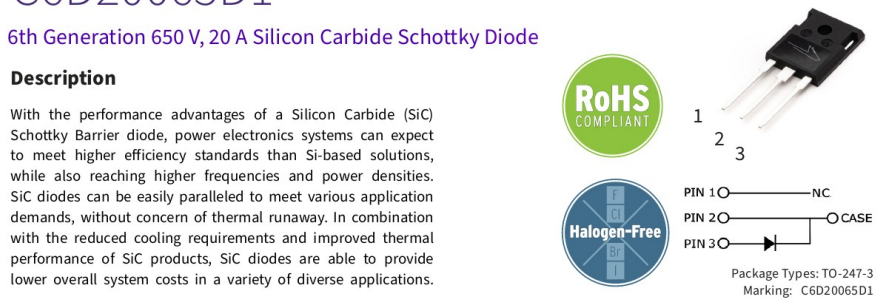
6. Power Module Design 2: Simulations

Simulation example of **DISCRETE** Power Semiconductors: **LTspice Models**

LTSpice simulations with discrete Power Devices (eg. TO)

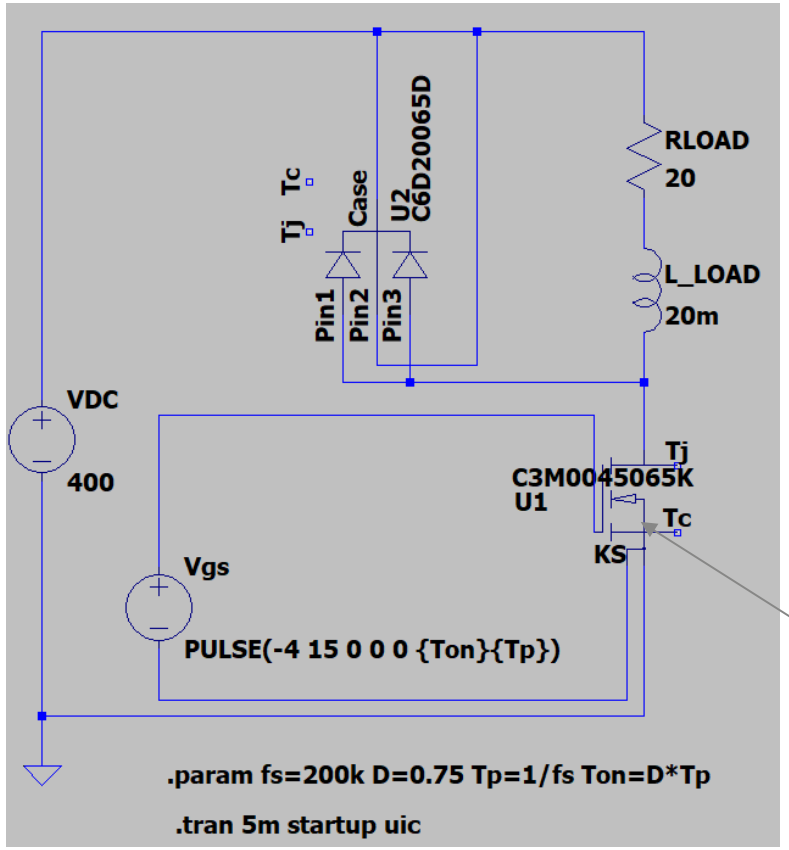
Discrete Semiconductors libraries: ex
https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/

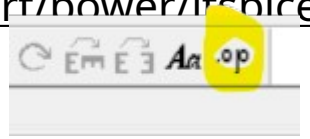




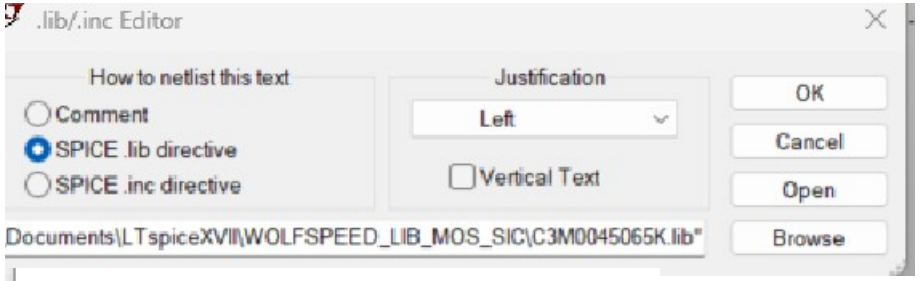
LTSpice simulations with discrete Power Devices (eg. TO)

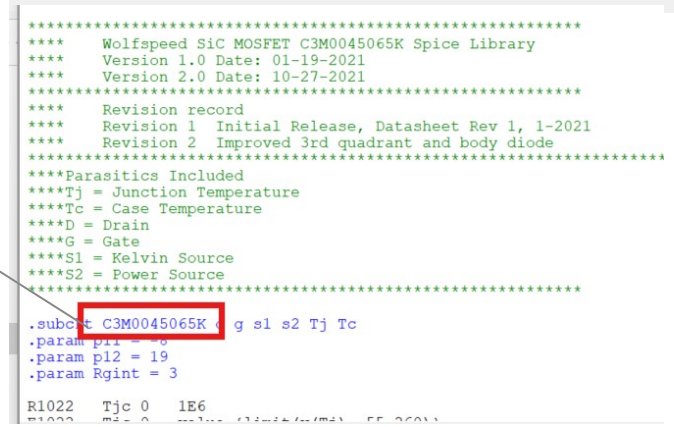
Discrete Semiconductors libraries: ex
https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/



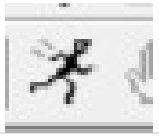


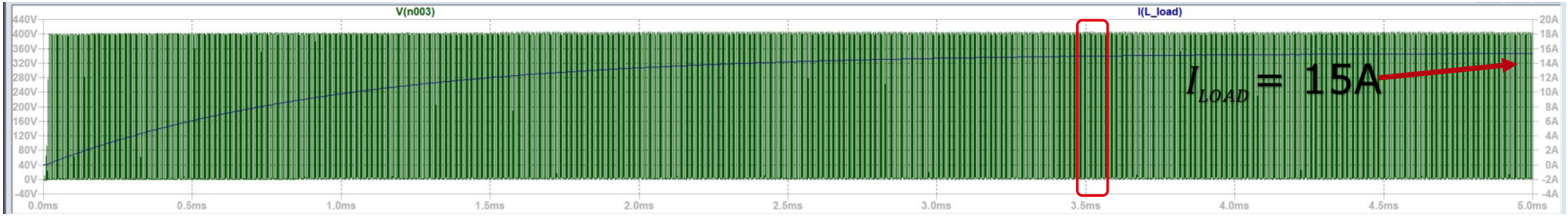
- right click

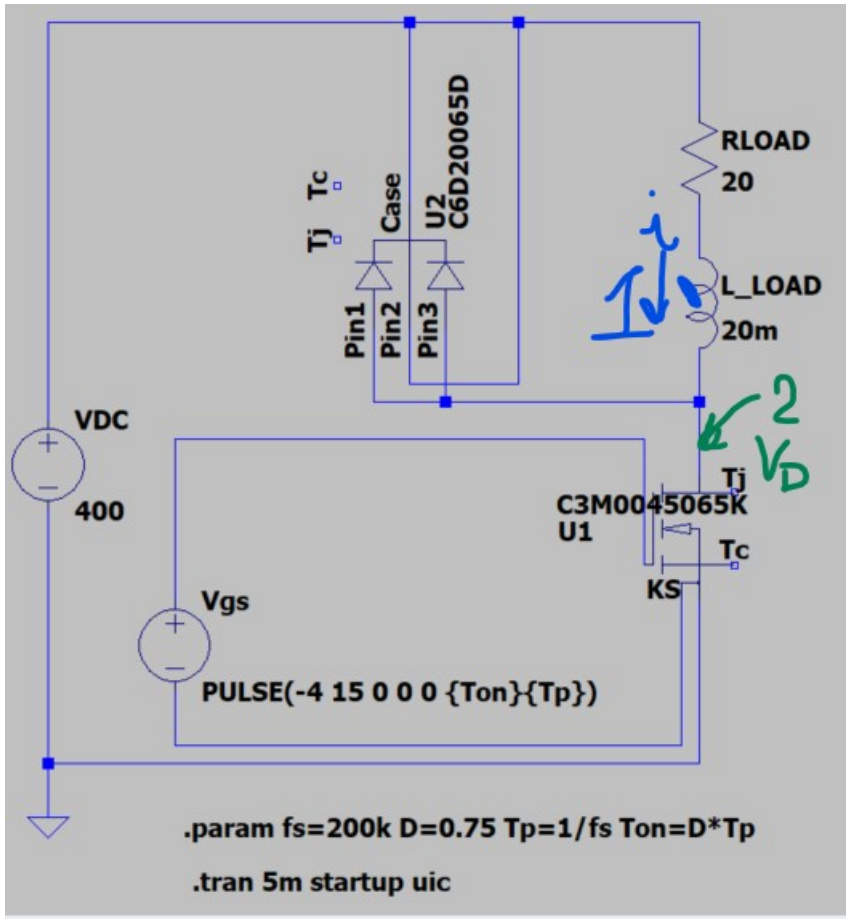


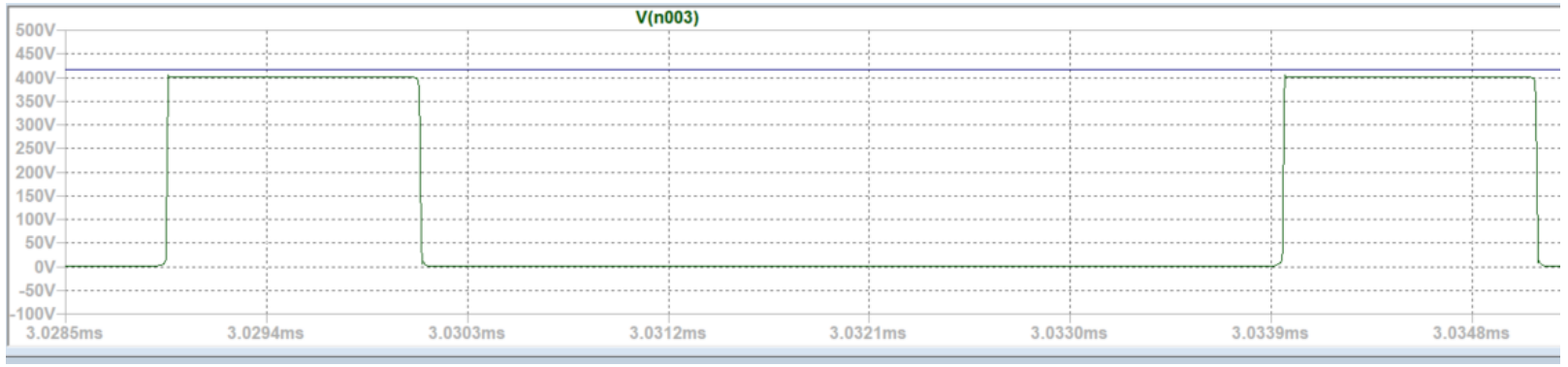


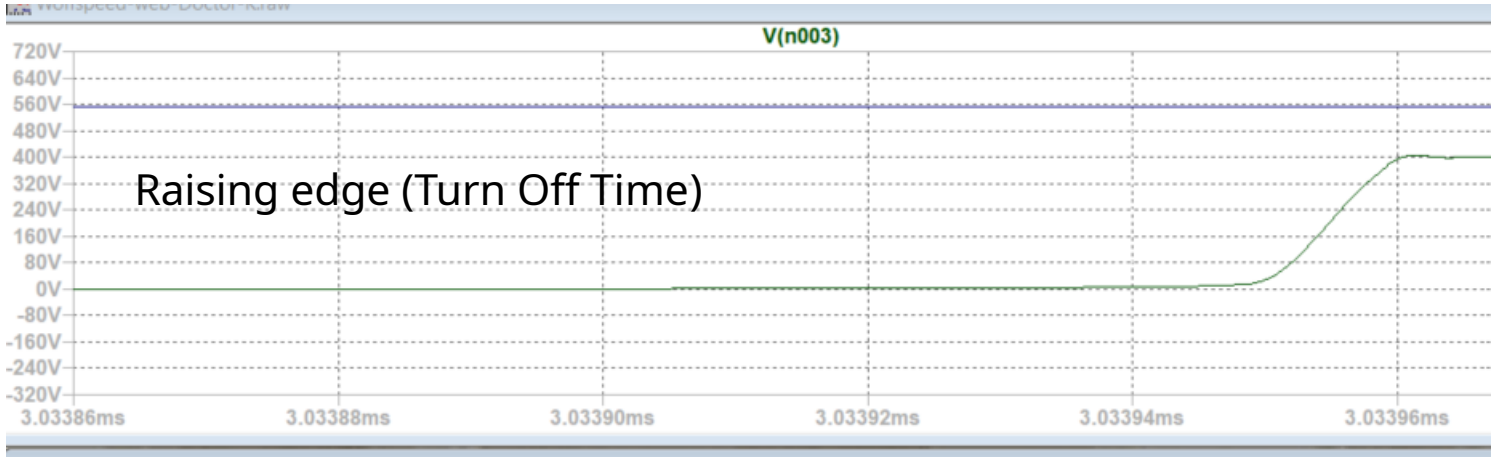
- The same for diode
- Make sure device name matches the library name!
- Then RUN



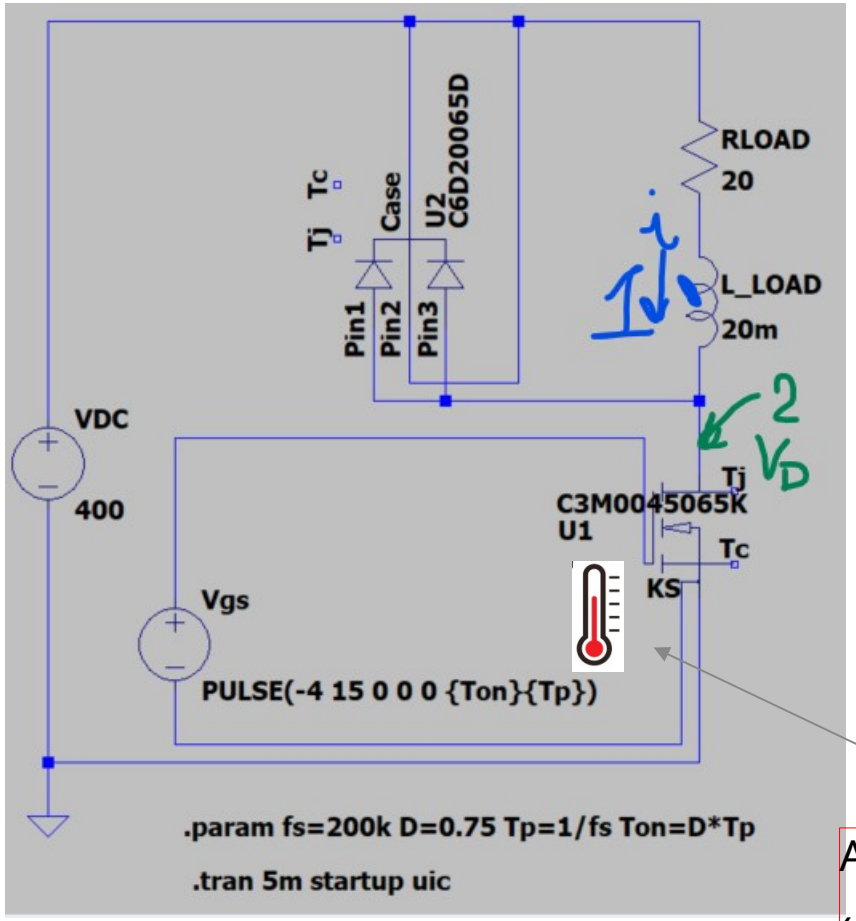


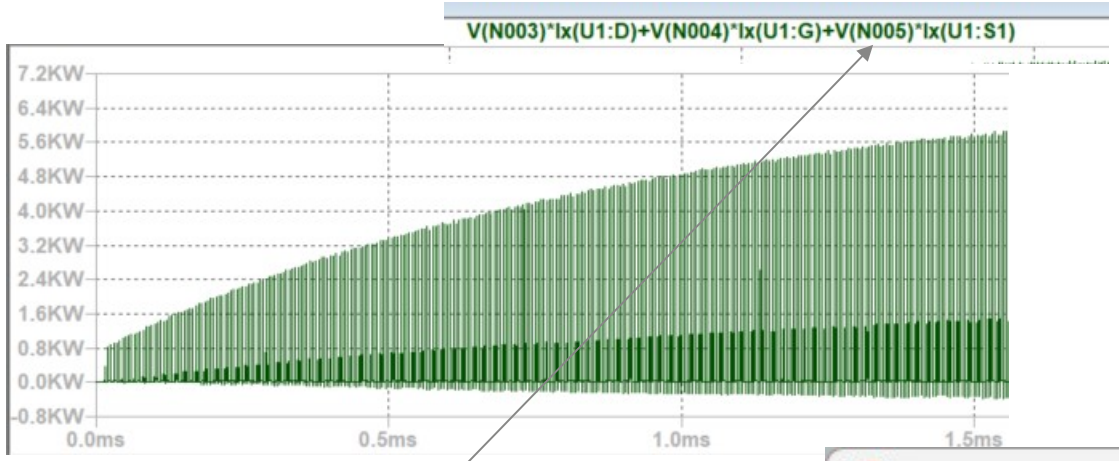


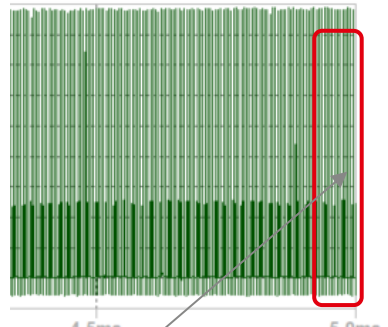




Dynamic Losses 1/2

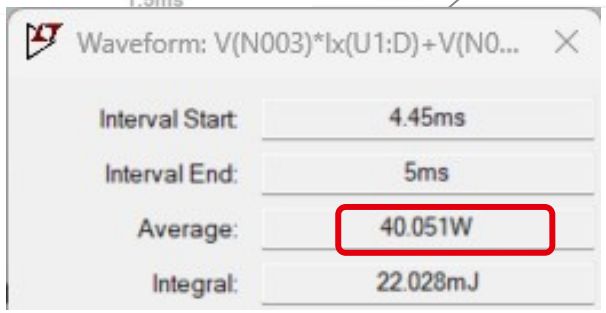






LEFTCLICK+CTRL: power consumption averaged over the selected range

(DEPEND by TIME RANGE)



40 Watt dissipated in the MOS:

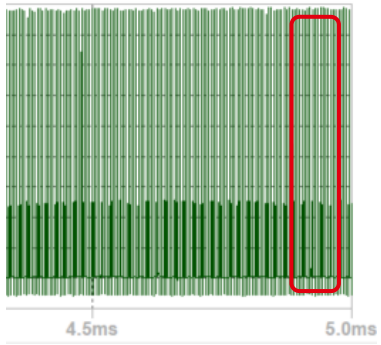
a lot?

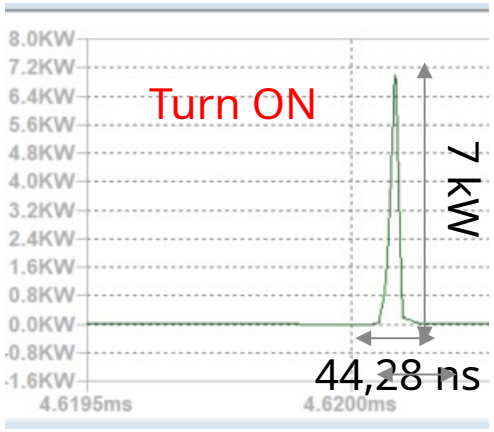
the **RLOAD** dissipate 400Vx15A → 4,5 kW! Only 40Watt dissipated over the power switch (1000 times less!)

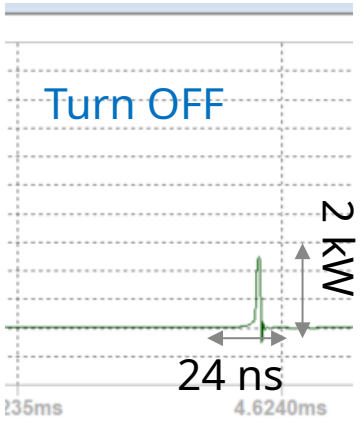
ALT+ probe

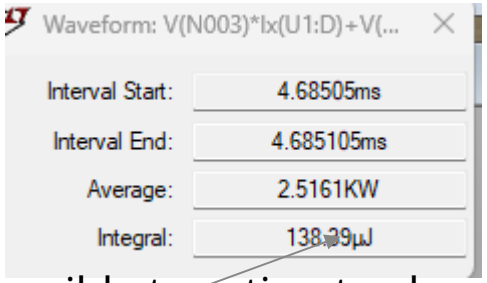
(probe power consumption)

Dynamic Losses 2/2









- possible to estimate also graphically (zoom on Turn on , Left cick + CTRL on title (not very accurate)

$$E_{on} = \frac{44{,}28 \times 7 \times 10^{-9} \times 10^{3}}{2} = 155\mu J \qquad E_{OFF} = \frac{24 \times 2 \times 10^{-9} \times 10^{3}}{2} = 24\mu J$$

Warning : Datasheet Turn ON / OFF calculated differenlty!

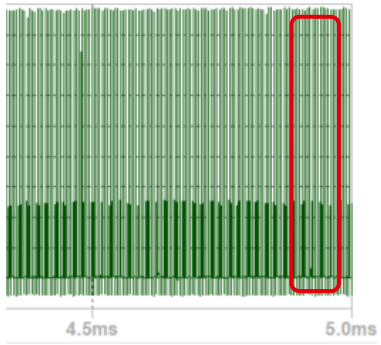
C3M0045065K

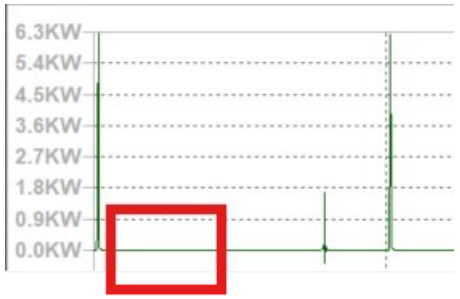
Turn-On Switching Energy (Body Diode)	E_{on}	—	57	—	µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 17.6 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET
Turn Off Switching Energy (Body Diode)	E_{off}	—	14	—		

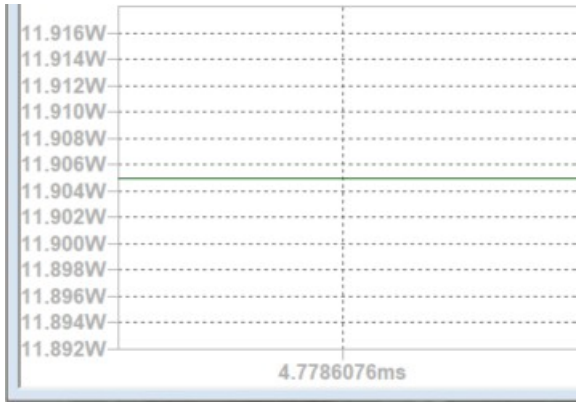
Fig.

Excercise: explain why this difference from semiconductor's physics concepts

Conduction Losses







Need to zoom a lot! → 11,9 W

Multiplied by the duty cycle=0.75 → 8,925 W

What is $R_{DS(ON)}$? → $W_{on} = V_{on} I_{on} = R_{DS(ON)} I_{on}^2 = 8{,}925W$

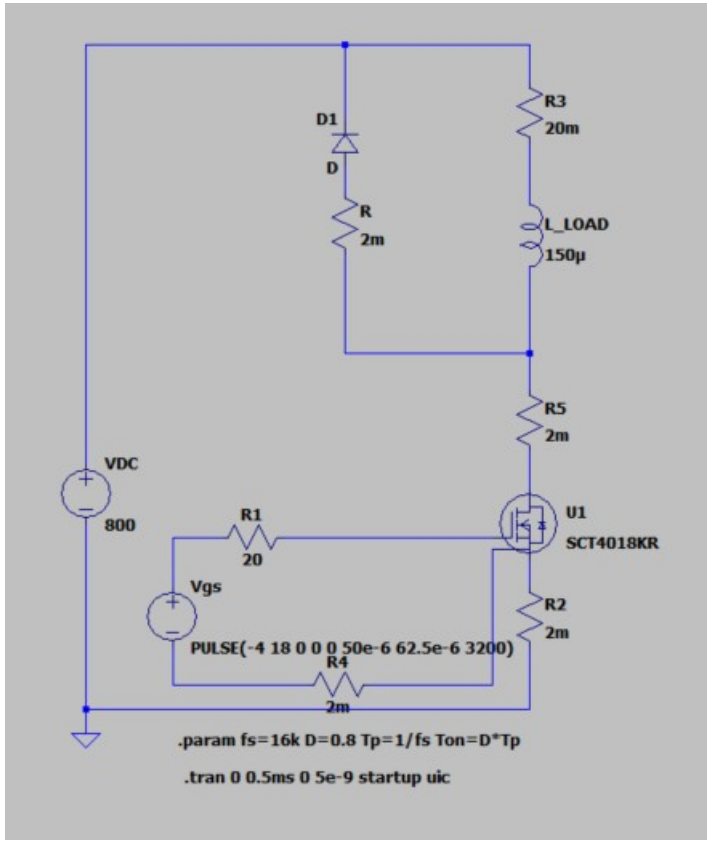
$I_{LOAD} = 15A$

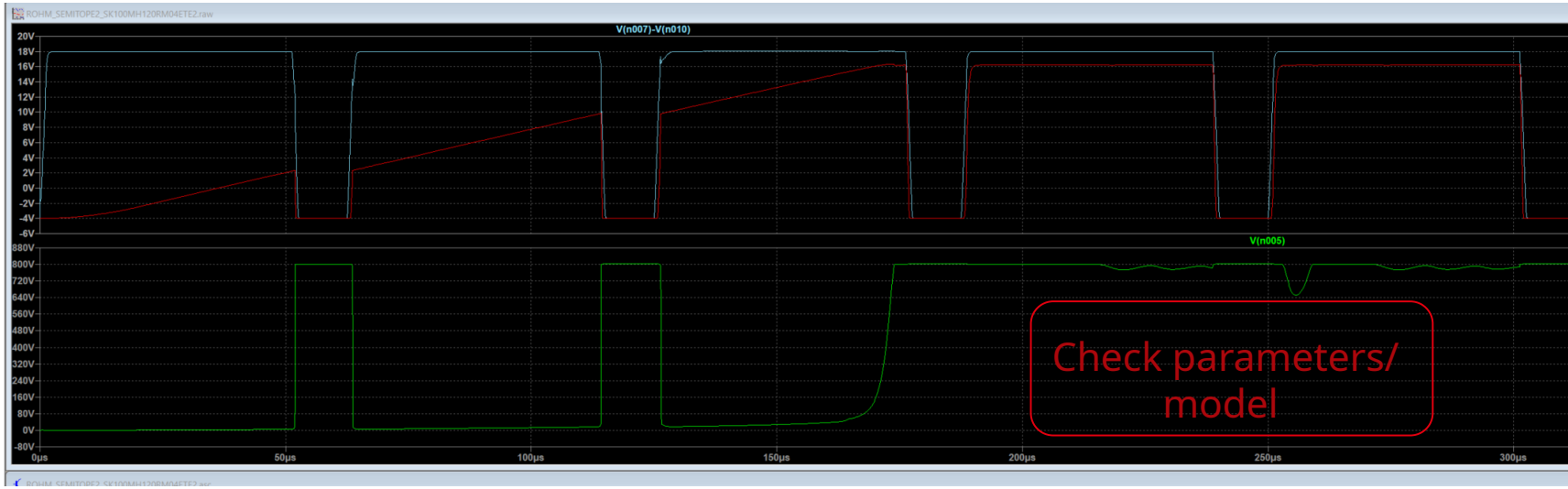
$$R_{DS(ON)} = \frac{8{,}925}{15^2} = \frac{8{,}925}{225} = 0.039 = 40m\Omega$$

Check datasheet: ok (Typical is +/- 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source On-State Resistance	$R_{DS(on)}$	—	45	60	mΩ	V_{GS} = 15 V, I_D = 17.6 A	Fig. 4, 5, 6
		—	61	—		V_{GS} = 15 V, I_D = 17.6 A, T_J = 175°C	

Esercizio





ROHM SEMICONDUCTOR

SCT4018KR

N-channel SiC power MOSFET Datasheet

V_{DSS}	1200V
$R_{DS(on)}$ (Typ.)	18mΩ
I_D *1	81A
P_D	312W

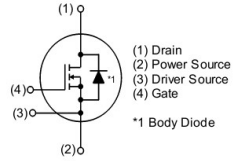
● Features

1) Low on-resistance
2) Fast switching speed
3) Fast reverse recovery
4) Easy to parallel
5) Simple to drive

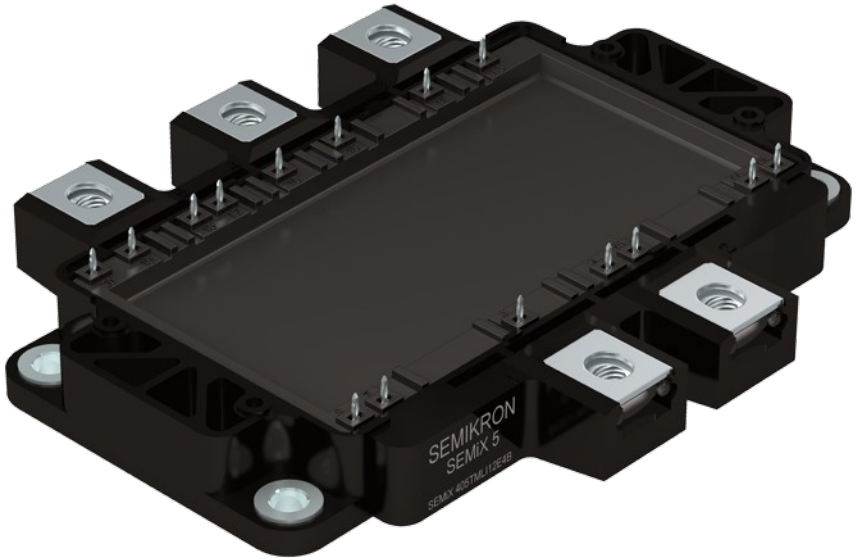
●Outline

TO-247-4L

●Inner circuit



Simulation example of POWER Semiconductor **MODULE SEMISEL**



Feasibility Details

Immaginiamo che il nostro cliente voglia usare un modulo di potenza come **convertitore per applicazioni fotovoltaiche**. Alla fine della prima fase di discussione bisognerà quindi avere chiarito

1. Il livello di tensione di ingresso
2. La corrente media di uscita o RMS (si parla sempre di corrente medie nell'ambito della conversione della energia per grandezze sinusoidali: Il mondo esterno è a 50Hz o 60Hz!)
3. Il cosφ (per applicazioni solari è 1)[3]
4. La frequenza della rete di uscita (in USA 60Hz, in Europa 50Hz) : stiamo progettando un convertitore che fornisce una tensione continua dal sistema fotovoltaico e che dovrà allacciarsi su una tensione di rete alternata.
5. La frequenza di switching del convertitore (switching frequency) perché come sapete la conversione di energia a semiconduttori si fa con le tecniche di switching.
6. La potenza di uscita richiesta (per un modulo di media potenza può essere 250 kW)

1. Circuit Parameter

DC/AC: 3 Level NPC

1.1 Nominal Load

Input voltage (V_{in}) 1250 V	Output voltage (V_{out}) 600 Vrms
Output current (I_{out}) 240 Arms	Output power (P_{out}) 249.42 kW
cos(φ) 1	Output frequency (f_{out}) 60 Hz
Switching frequency (f_{sw}) 6 kHz	Modulation Sinus triangle PWM

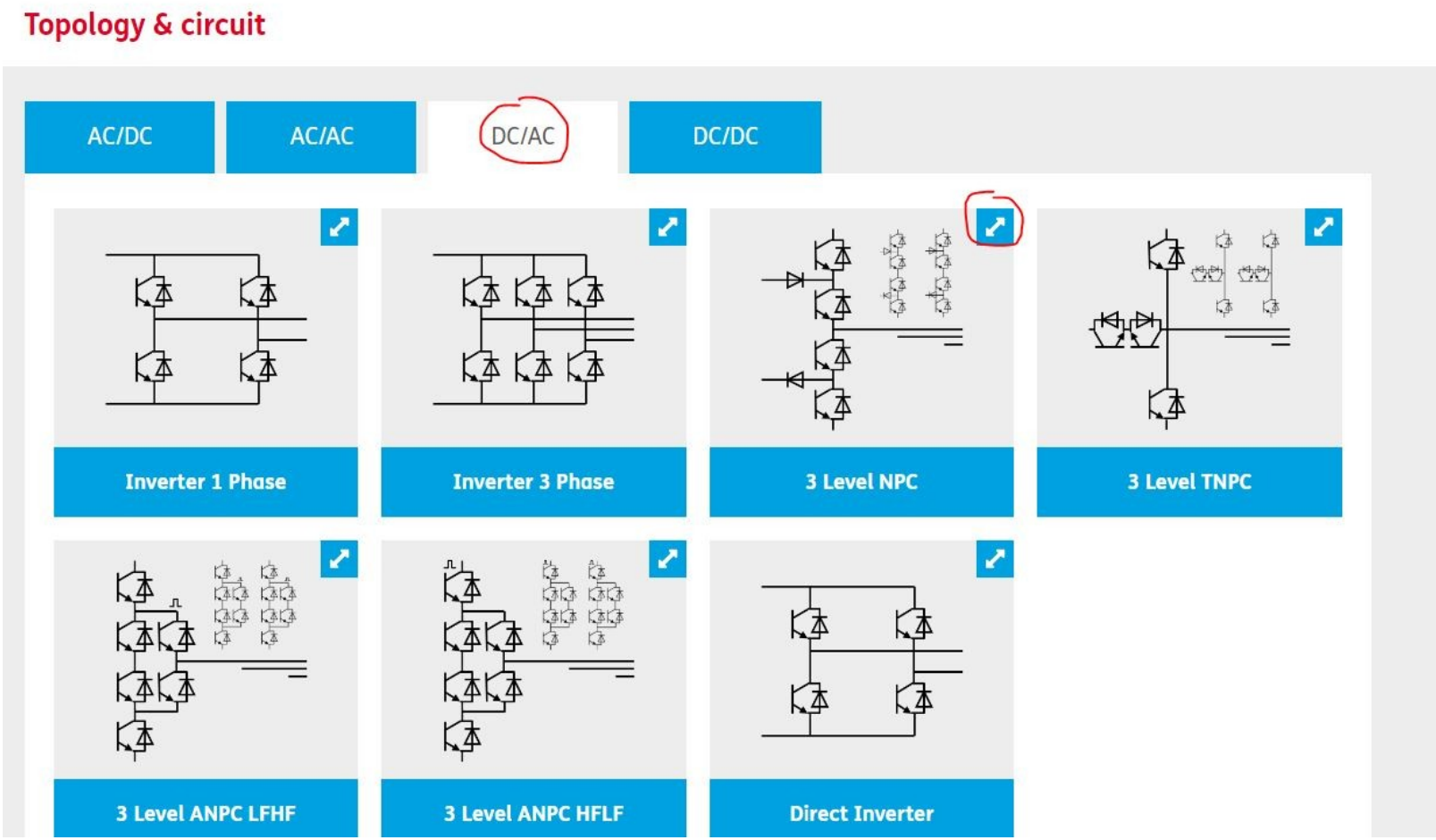
Figura 2.4: Esempio di parametri elettrici per un Modulo di Potenza per applicazioni fotovoltaiche

[3]Questo è un obiettivo. Stiamo progettando un inverter fotovoltaico che deve generare una tensione alternata da immettere in rete e deve convertire quindi la potenza solare in potenza di rete introducendo la più piccola distorsione armonica quindi cercando di riuscire a generare tensioni e correnti perfettamente in fase. Questo perché esistono delle normative entro cui il sistema fotovoltaico può scambiare energia reattiva con la rete e questo non deve essere inferiore a 0.8. Soprattutto perché il distributore valuta (e fattura) la potenza «ATTIVA» prodotta o consumata (e NON quella «reattiva»). Infine quando l'impianto non è attivo (di notte) l'inverter deve comportarsi come un'utenza passiva. Generazione o consumo di energia in impianti solari in ore notturne NON sono permessi :-)

Example: Design Power Module for Photovoltaic DC/AC application. Project Simulation: SEMISEL 1/7

SemiSel Simulation | Semikron Danfoss

Define the Topology and Circuit…



Example: Design Power Module for Photovoltaic DC/AC application. Project Simulation: SEMISEL 2/7

define the Input parameters ...

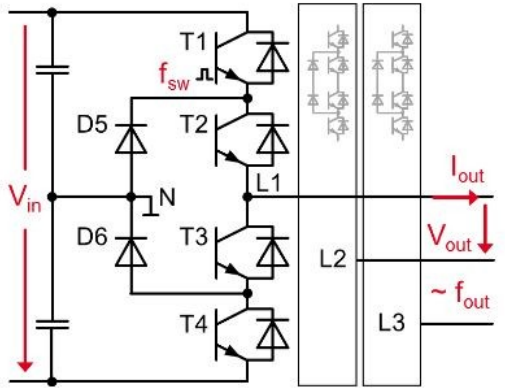
◂ Topology & circuit

Product selection ▸

Nominal load

Input voltage (V_{in})	1250 V	Output voltage (V_{out})	600 Vrms
Output current (I_{out})	240 Arms	Output power (P_{out})	249 kW
Power factor (cos φ)	1	Output frequency (f_{out})	60 Hz
Switching frequency (f_{sw})	6 kHz	Modulation (M)	Sinus triangle PWM
Additional losses per heatsink (P_{+HS})	0 W		

Circuit: 3 Level NPC - DC/AC



Example: Design Power Module for Photovoltaic DC/AC application. Project Simulation: SEMISEL 3/7

SEMiX305MLI12E4V2 seems to be a module which matches the specifications.

Let's verify if this module work under the specific conditions requested by the application

SEMiX305MLI12E4V2

SEMiX® 5

3-Level NPC IGBT-Module

SEMiX305MLI12E4V2

Features*

- Solderless assembling solution with PressFIT signal pins and screw power terminals
- IGBT 4 Trench Gate Technology
- $V_{CE(sat)}$ with positive temperature

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
IGBT1				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 175 °C	T_c = 25 °C	451	A
		T_c = 80 °C	347	A
I_{Cnom}			300	A
I_{CRM}			900	A
V_{GES}			-20 ... 20	V
t_{psc}	V_{CC} = 800 V, V_{GE} ≤ 15 V, T_j = 150 °C, V_{CES} ≤1200 V		10	µs
T_j			-40 ... 175	°C
IGBT2				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 175 °C	T_c = 25 °C	453	A
		T_c = 80 °C	348	A
I_{Cnom}			300	A
I_{CRM}			900	A
V_{GES}			-20 ... 20	V
t_{psc}	V_{CC} = 800 V, V_{GE} ≤ 15 V, T_j = 150 °C, V_{CES} ≤ 1200 V		10	µs
T_j			-40 ... 175	°C
Diode1				

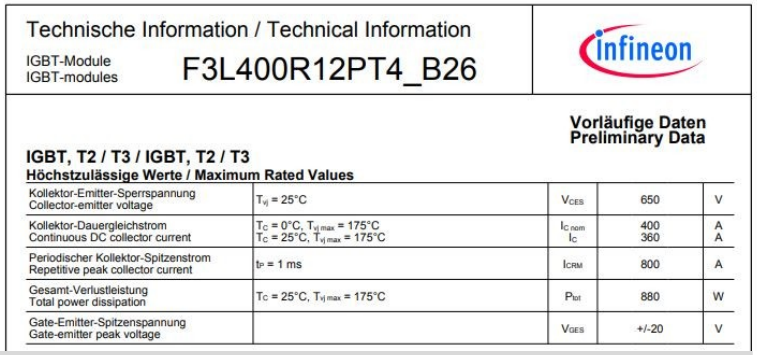
Example: Design Power Module for Photovoltaic DC/ACapplication. Project Simulation: SEMISEL 4/7

Cooling

Once chosen the defined module we must chose the cooling system

For IGBT4 with Tj,op=150°C a possible cooling temperature in stationary state can be 98°C

... based on real (?) case ☺



Technische Information / Technical Information

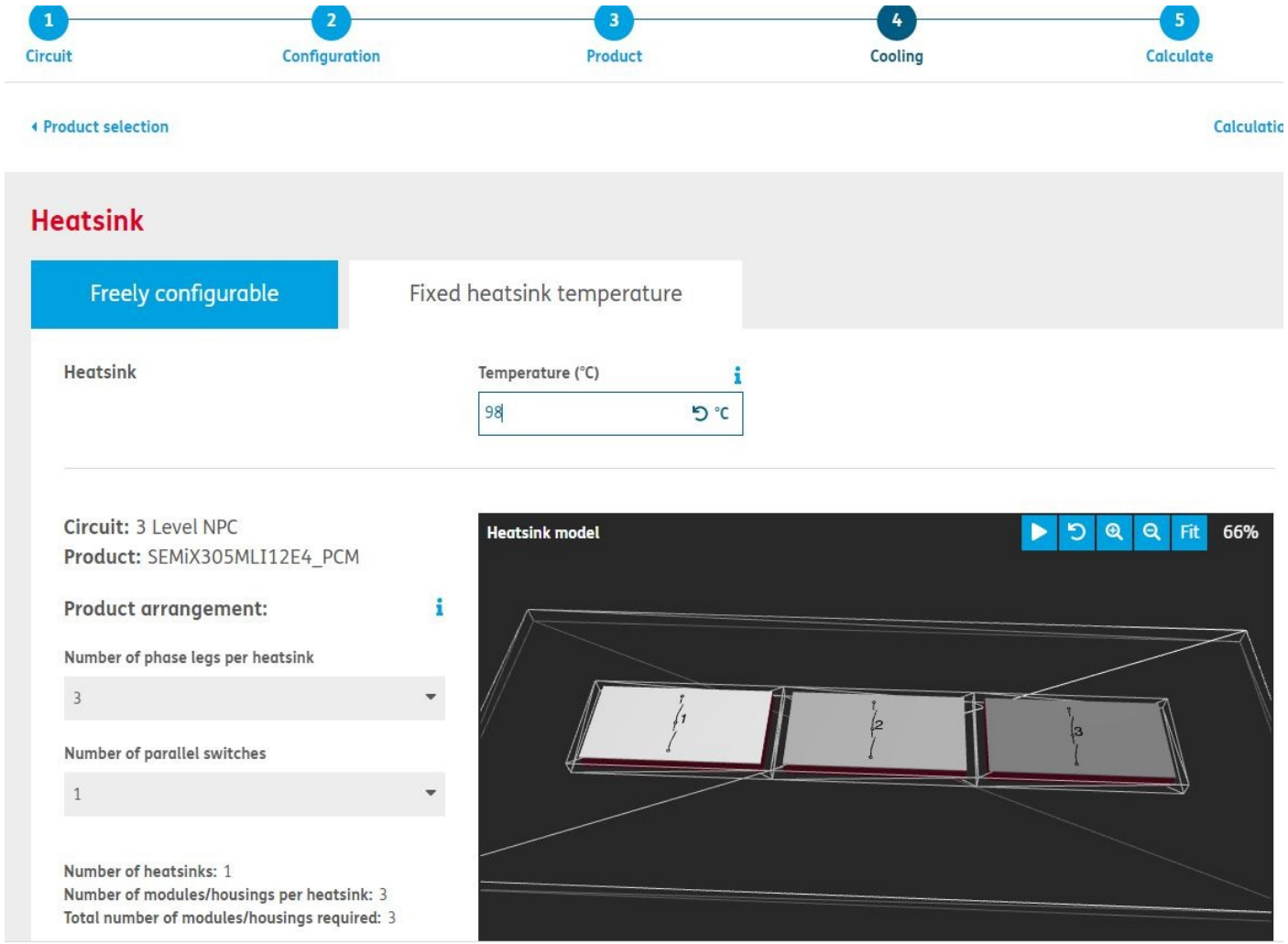
IGBT-Module
IGBT-modules

F3L400R12PT4_B26

Vorläufige Daten
Preliminary Data

IGBT, T2 / T3 / IGBT, T2 / T3
Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C	V_{CES}	650	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 0°C, $T_{vj\,max}$ = 175°C T_C = 25°C, $T_{vj\,max}$ = 175°C	$I_{C\,nom}$ I_C	400 360	A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	800	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 175°C	P_{tot}	880	W
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V



Example: Design Power Module for Photovoltaic DC/AC application. Project Simulation: SEMISEL 5/7

Product Selection …

- Possibility to customize some key static and dynamic losses for the product selection

- Static losses $\propto V_{CE0}, T_j$

  $\frac{1}{\propto} R_{th}, r_{CE}$

$$I_C\left(T_{case}\right) = \frac{-V_{CE(0)}}{2 \cdot r_{CE}} + \sqrt{\left(\frac{V_{CE(0)}}{2 \cdot r_{CE}}\right)^2 + \frac{T_{Jmax} - T_{case}}{R_{th(j-c)} \cdot r_{CE}}}$$

- Thermal Resistances

- Dynamic Losses

SEMiX305MLI12E4V2

SEMiX® 5

3-Level NPC IGBT-Module

SEMiX305MLI12E4V2

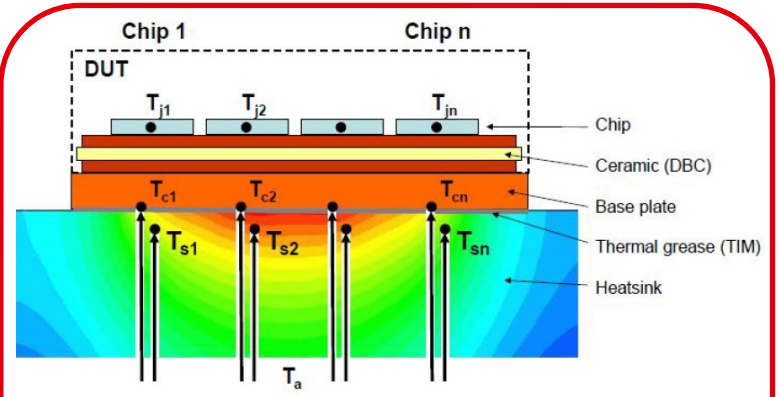
Features*

- Solderless assembling solution with PressFIT signal pins and screw power terminals
- IGBT 4 Trench Gate Technology
- $V_{CE(sat)}$ with positive temperature coefficient
- Low inductance case
- Reliable mechanical design with injection moulded terminals and reliable internal connections
- UL recognized file no. E63532
- NTC temperature sensor inside

Static Losses

Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
IGBT1						
$V_{CE(sat)}$	I_C = 300 A, V_{GE} = 15 V, chiplevel	T_j = 25 °C		1.80	2.05	V
		T_j = 150 °C		2.20	2.40	V
V_{CE0}	chiplevel	T_j = 25 °C		0.80	0.90	V
		T_j = 150 °C		0.70	0.80	V
r_{CE}	V_{GE} = 15 V, chiplevel	T_j = 25 °C		3.3	3.8	mΩ
		T_j = 150 °C		5.0	5.3	mΩ
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 12 mA		5	5.8	6.5	V
I_{CES}	V_{GE} = 0 V, V_{CE} = 1200 V, T_j = 25 °C				4.0	mA
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V	f = 1 MHz		18.6		nF
C_{oes}		f = 1 MHz		1.16		nF
C_{res}		f = 1 MHz		1.02		nF
Q_G	V_{GE} = -8V...+15V			1700		nC
R_{Gint}	T_j = 25 °C			2.5		Ω
$t_{d(on)}$	V_{CC} = 600 V, I_C = 300 A, V_{GE} = +15/-8 V, $R_{G\,on}$ = 0.5 Ω	T_j = 150 °C		71		ns
t_r		T_j = 150 °C		51		ns
E_{on}		T_j = 150 °C		17.4		mJ
$t_{d(off)}$	$R_{G\,off}$ = 1.5 Ω	T_j = 150 °C		488		ns
t_f	di/dt_{on} = 5700 A/µs, di/dt_{off} = 2300 A/µs, dv/dt = 3500 V/µs	T_j = 150 °C		148		ns
E_{off}		T_j = 150 °C		38.7		mJ
$R_{th(j-c)}$	per IGBT				0.1	K/W
$R_{th(c-s)}$	per IGBT (λgrease=0.81 W/(m*K))			0.077		K/W
$R_{th(c-s)}$	per IGBT, pre-applied phase change material			0.037		K/W



Dynamic Losses

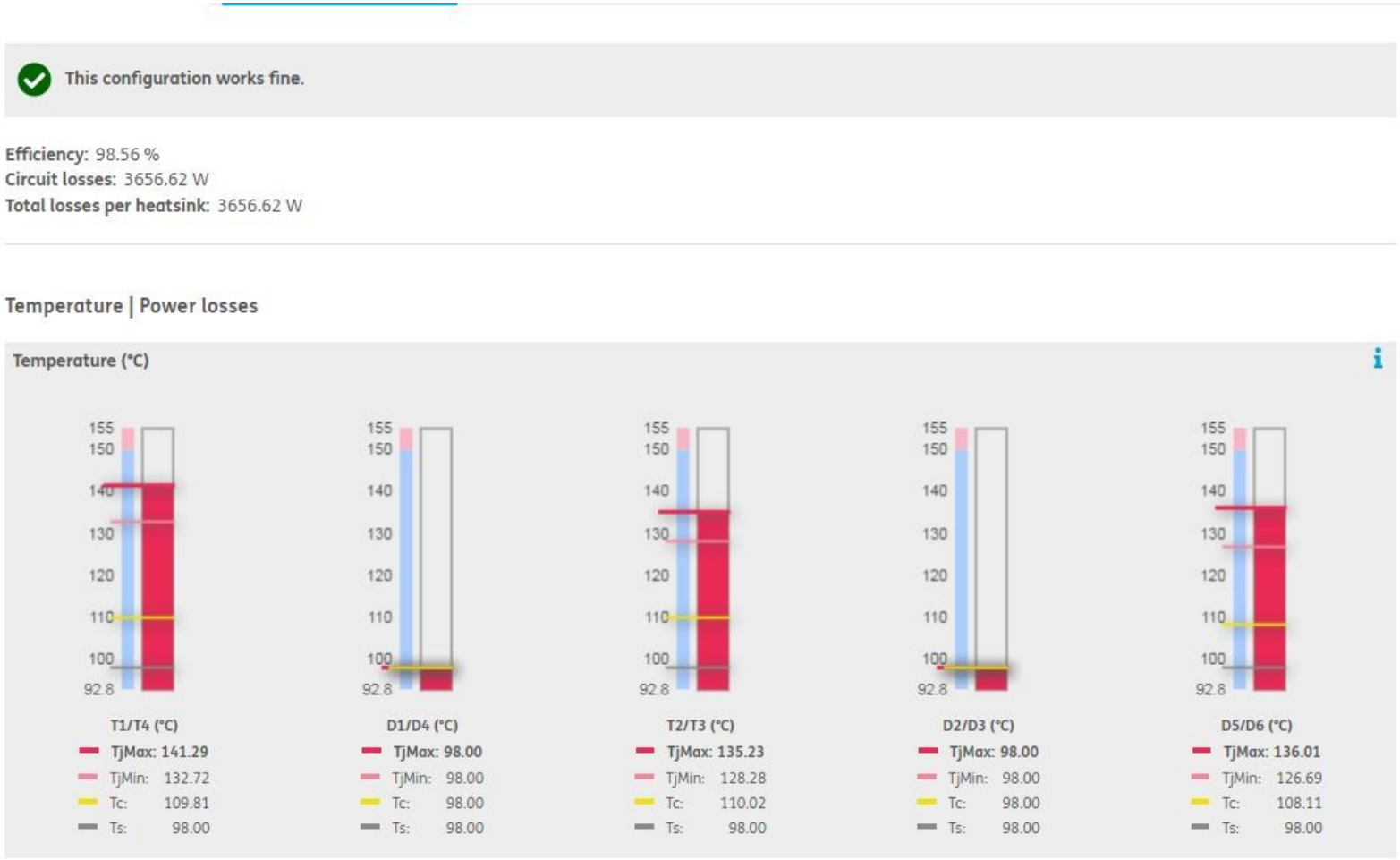
Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
IGBT1						
$t_{d(on)}$	V_{CC} = 600 V, I_C = 300 A, V_{GE} = +15/-8 V, $R_{G\,on}$ = 0.5 Ω	T_j = 150 °C		71		ns
t_r		T_j = 150 °C		51		ns
E_{on}		T_j = 150 °C		17.4		mJ
$t_{d(off)}$	$R_{G\,off}$ = 1.5 Ω	T_j = 150 °C		488		ns
t_f	di/dt_{on} = 5700 A/µs, di/dt_{off} = 2300 A/µs, dv/dt = 3500 V/µs	T_j = 150 °C		148		ns
E_{off}		T_j = 150 °C		38.7		mJ

Example: Design Power Module for Photovoltaic DC/AC application. Project Simulation: SEMISEL 6/7

Simulation outputs

Junction Temperatures under working conditions

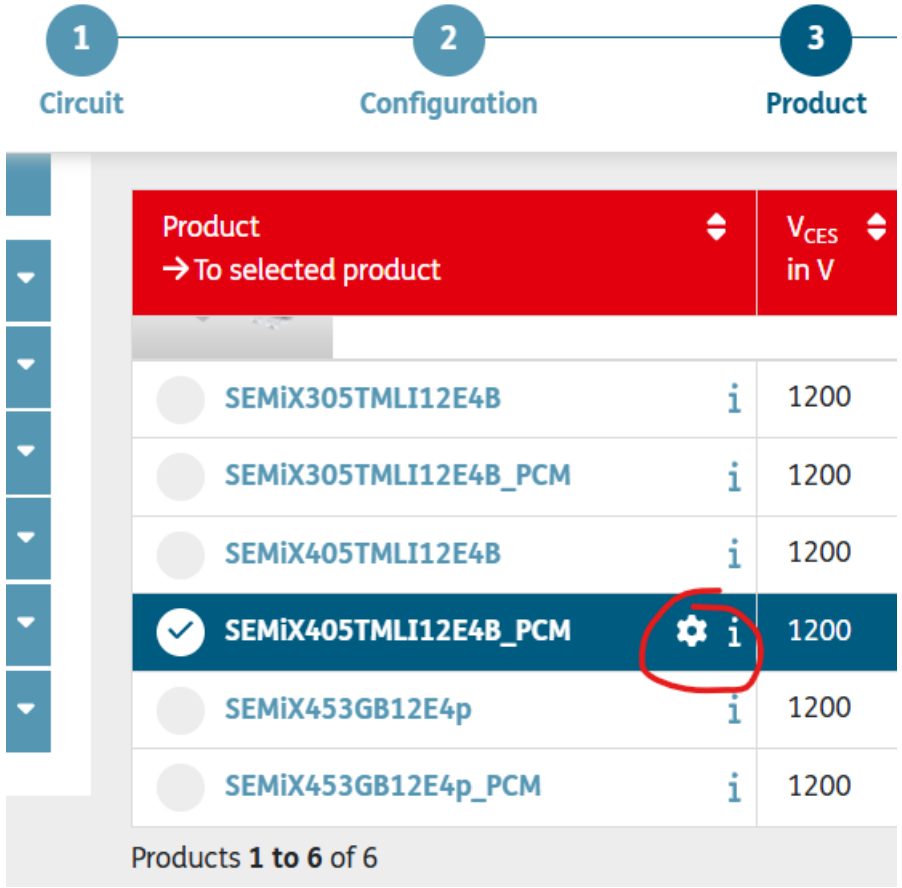


Example: Design Power Module for Photovoltaic DC/AC application. Project Simulation: SEMISEL 7/7

Simulation outputs

Power Losses under working conditions

Datasheet characteristics can be customized (useful for power module comparison)



Typical values | Maximum values

		T1/T4	D1/D4	T2/T3	D2/D3
I_{ref}	(A)	400	400	400	400
V_{ref}	(V)	300	300	300	300
$T_{j\,op}$	(°C)	150	150	150	150
$T_{j\,max}$	(°C)	175	175	175	175
$V_{f\,@\,25°C,\,Iref}$	(V)	1.8	2.2	1.55	1.39
$V_{f\,@\,Tjop,\,Iref}$	(V)	2.2	2.15	1.75	1.38
Rg_{On}	(Ohm)	2.5		0.5	
Rg_{Off}	(Ohm)	1.5	0.5	0.5	2.5
E_{on}	(mJ)	21.4		2.8	
E_{off}	(mJ)	29	16.4	23.9	7.8
$R_{th(j-c)}$	(K/W)	0.068	0.13	0.14	0.18
$R_{th(c-s)}$	(K/W)	0.015	0.028	0.046	0.046
$R_{th(c-s)\,per\,Module}$	(K/W)	0.006			

Semisel exercise: Power Module comparison (facile)

Make a comparison between this module

https://www.semikron-danfoss.com/products/p/semix405tmli12e4b-21919490

https://www.mitsubishielectric.com/semiconductors/powerdevices/datasheets/igbt/t_series/cm400st-24t_e.pdf

1) which type of chips are used for each switch?

hints : for SEMiX5 IGBT look here https://www.infineon.com/cms/en/product/power/igbt/

For SEMiX5 Diode look here:

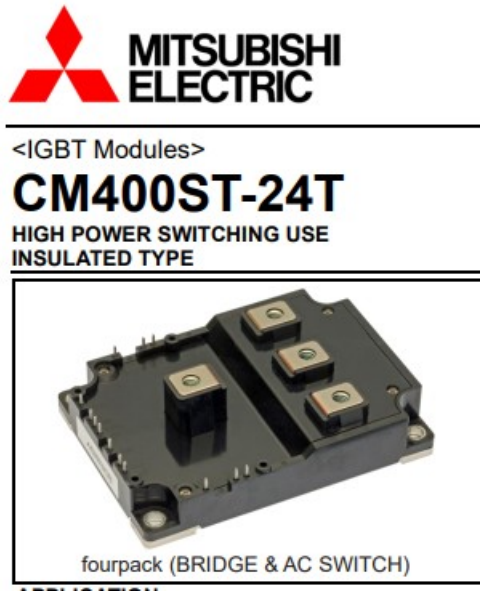
https://www.semikron-danfoss.com/products/bare-dies/freewheeling-diodes

for Mitsubishi look here: https://www.mitsubishielectric.com

2) based on the datasheet of power modules which modules could have bigger chips inside? Explain why you reached these conclusion

3) Make a comparison with Semisel of the two modules for a typical UPS application (Input Voltage: 800Vm Output current 350Arms, Fswitch 5Khz)

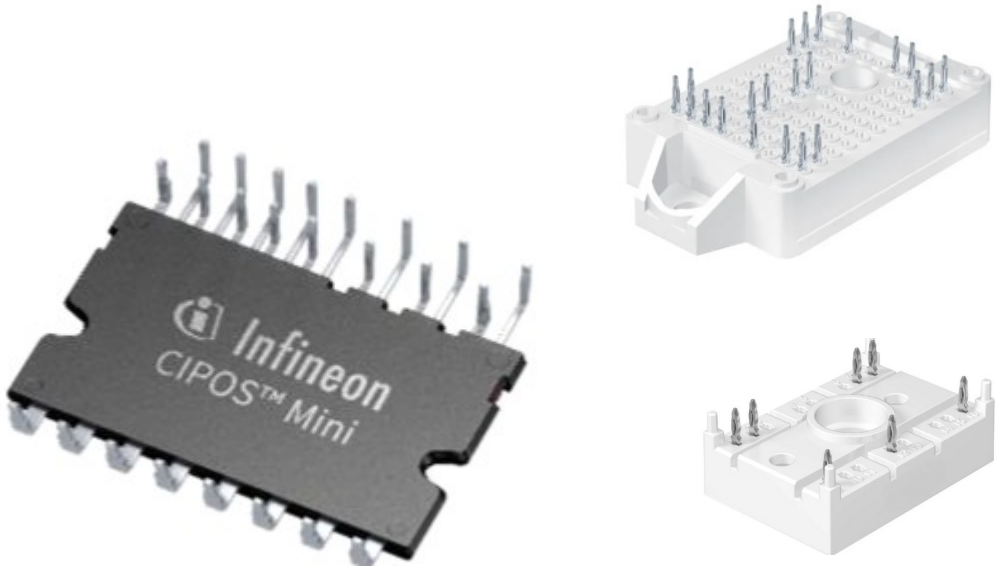
4) Explain the difference of the power losses make assumption on the internal chipset and/or other internal packaging/manufacturing dependencies.



Semisel exercise2: Power Module comparison (marketing) (difficile)

Make a research on www.semikron-danfoss.com website (specifically for SEMITOP CLASSIC, SEMITOP E1 or SEMITOP E2 and find a product which has similar performances on this one (at same voltage ,nominal current and power level)

https://www.infineon.com/dgdl/Infineon-IM06B20AC1-DataSheet-v01_20-EN.pdf?fileId=8ac78c8c92bcf0b0019368a29d805f6e



- Evaluate the losses between the two product
- Evaluate the thermal losses based on a typical motor drive application (use 5Khz of switching frequency)
- When the module is convenient for drive application (is there a breakeven for power for instance?) : try to make a sort of “fighting guide” (pro/cons DIP-IPM vs Module) based on some technical KPI for power electronics
- Estimate the “cost” to have this product embedded in a servo drive.

- 650 V TRENCHSTOP™ IGBT7 T7

3.2 Inverter section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{CES}		650	V
DC link supply voltage of P-N	V_{PN}	Applied between P-N	450	V
DC link supply voltage (surge) of P-N	$V_{PN\ (surge)}$	Applied between P-N	500	V
Output current[2]	I_O	T_C = 25°C, T_J < 150°C	±20	A
		T_C = 80°C, T_J < 150°C	±15	
Maximum peak output current	$I_{O\ (peak)}$	T_C = 25°C, T_J < 150°C less than 1 ms	±40	A
Power dissipation per IGBT	P_{tot}		32.05	W
Short circuit withstand time	t_{SC}	V_{DC} ≤ 360V, T_J = 150°C	3	µs

Customization vs full re-design

- Check if available modules fits the customer application (design effort is zero)
- First level of design : chip customization (reiterate simulation with static and dynamic losses from similar packages)
- If Semisel cannot found a suitable module even with small chip change we need for a full custom design. Critical parameters need to be reviewed

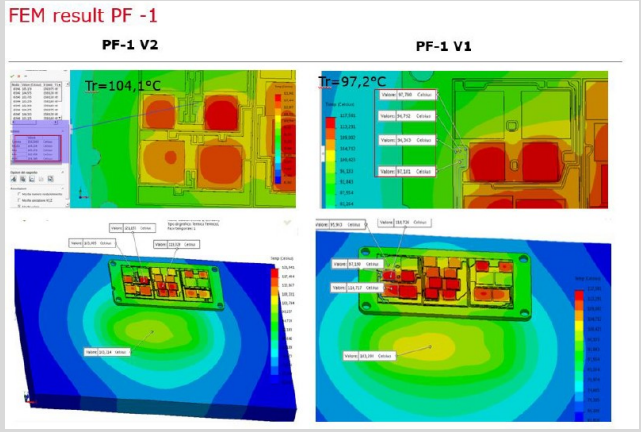
a. Where losses comes from? Inductances → Over voltages

$$\nabla V = L \cdot \frac{di}{dt}$$

$$\Phi(\vec{B}) = LI$$

$$L = \mu_0 n^2 l S$$

-----→ Geometry dependant! → DCB re-layout?



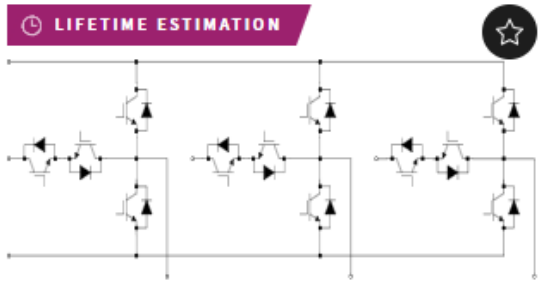
- Temperature heat flow? FEM simulation to evaluate packaging performances?

Simulation example of POWER Semiconductor **MODULE IPOSIM**

https://www.infineon.com/design-resources/simulation-modeling/iposim-infineon-power-simulation-tool-plecs

DC/AC

DC/AC Applications



Filter Devices

Circuit configuration: Single switch

Half DC link voltage $V_{DC}/2$: 325 V

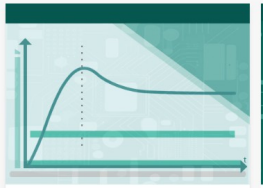
Blocking voltage: 1200 (recommended)

Rated current: 340 A

Filter by packaging: All

Device Name	TIM	Package	V_{CES}/V_{DSS} [V]	I_{Cnom}/I_{Dnom} [A]	$V_{CEsat, 125°C}/V_{DSsat, 125°C}$ [V]	$E_{on} + E_{off,125°C}$ [mWs]	R_{th} [K/W]	T_{vjmax} [°C]
FZ400R12KE3	-	62mm ES	1200	400	2	92.00	0.07	125
FZ400R12KE4	-	62mm ES	1200	400	2	83.00	0.08	150

Next →



Circuit & Control

Modulation algorithm: SPWM

Half DC link voltage $V_{DC}/2$: 325 V

Output current I_{out}: 350 Arms

Output frequency: 50 Hz

Switching frequency: 2000 Hz

Modulation index: 1

Power factor cos(ϕ): 1

Output voltage V_{out}: 398 V

Reactive power type: Inductive load (lagging)

Thermal

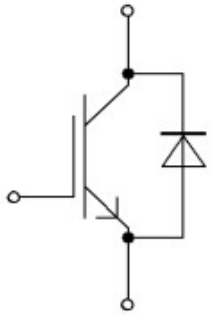
Heatsink model: Fixed heatsink temperature

Heatsink temperature T_h: 80 °C

Confirm / Run →

DC/AC

	MAXIMUM JUNCTION TEMPERATURE	CONDUCTION LOSSES	SWITCHING LOSSES	TOTAL LOSSES
SWITCH Q1/Q4	105.22 °C	246.39 W	31.43 W	277.81 W
DIODE D1/D4	80 °C	0.00 W	0.00 W	0.00 W
SWITCH Q2/Q3	84.65 °C	52.9 W	0 W	52.9 W
DIODE D2/D3	90.38 °C	48.24 W	14.09 W	62.33 W



V_{CES} = 1200V
$I_{C\,nom}$ = 400A / I_{CRM} = 800A

技术信息 / Technical Information

IGBT-模块
IGBT-modules

FZ400R12KE4

62mm C-Series 模块 采用第四代沟槽栅/场终止IGBT4和第四代发射极控制二极管
62mm C-Series module with Trench/Fieldstop IGBT4 and Emitter Controlled 4 diode

Simulation example of POWER Semiconductor **MODULE VINCOSIM**

https://www.vincotech.com/support-and-documents/simulation-software.html

Vincotech

TOPOLOGY | SUB-TOPOLOGY | PRODUCT LINE | VOLTAGE IN V | CURRENT IN A | MAIN CHIP TECHNOLOGY | HOUSING FAMILY | HEIGHT IN MM

DC/AC NPC

1. Circuit Parameter

DC/AC: 3 Level NPC

1.1 Nominal Load

Input voltage (V_{in}) 1250 V	Output voltage (V_{out}) 600 Vrms
Output current (I_{out}) 240 Arms	Output power (P_{out}) 249.42 kW
cos(φ) 1	Output frequency (f_{out}) 60 Hz
Switching frequency (f_{sw}) 6 kHz	Modulation Sinus triangle PWM

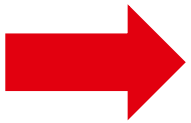


Figura 2.4: Esempio di parametri elettrici per un Modulo di Potenza per applicazioni fotovoltaiche

10-EY122PA005MS-LU39F78T	Samples available	Half-Bridge-NTC	flowDUAL E2 SiC	1200	290	SiC MOSFET	flow E2	12	Al_2O_3	REQUEST SIMULATION

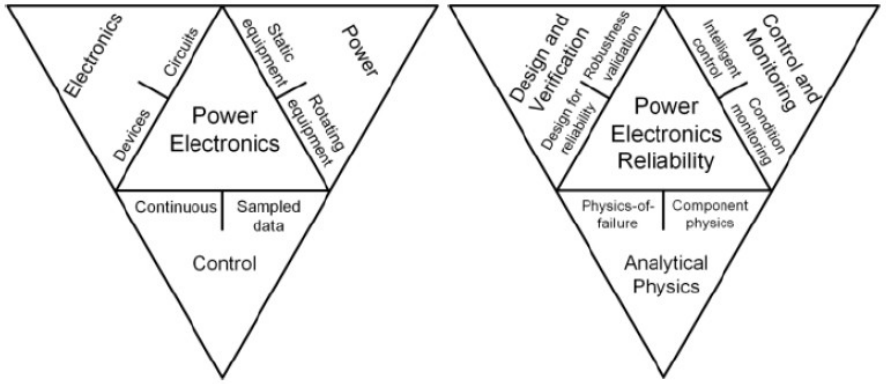
Power Electronics

7. Reliability

Design for Reliability

THE RELIABILITY CHALLENGE IN INDUSTRY SEEN BEFORE, TODAY AND IN THE FUTURE

	Yesterday	Today	Tomorrow
Customer expectations	– Replacement if failure – Years of warranty	– Low risk of failure – Request for maintenance	– Peace of mind – Predictive maintenance
Reliability target	– Affordable market returns (%)	– Low market return rates	– ppm market return rates
R&D approach	– Reliability test – Avoid catastrophes	– Robustness tests – Improve weakest components	– Design for reliability – Balance with field load / mission profile
R&D key tools	– Product operating and function tests	– Testing at the limits	– Understanding failure mechanisms, field load, root cause – Multi-domain simulation – …

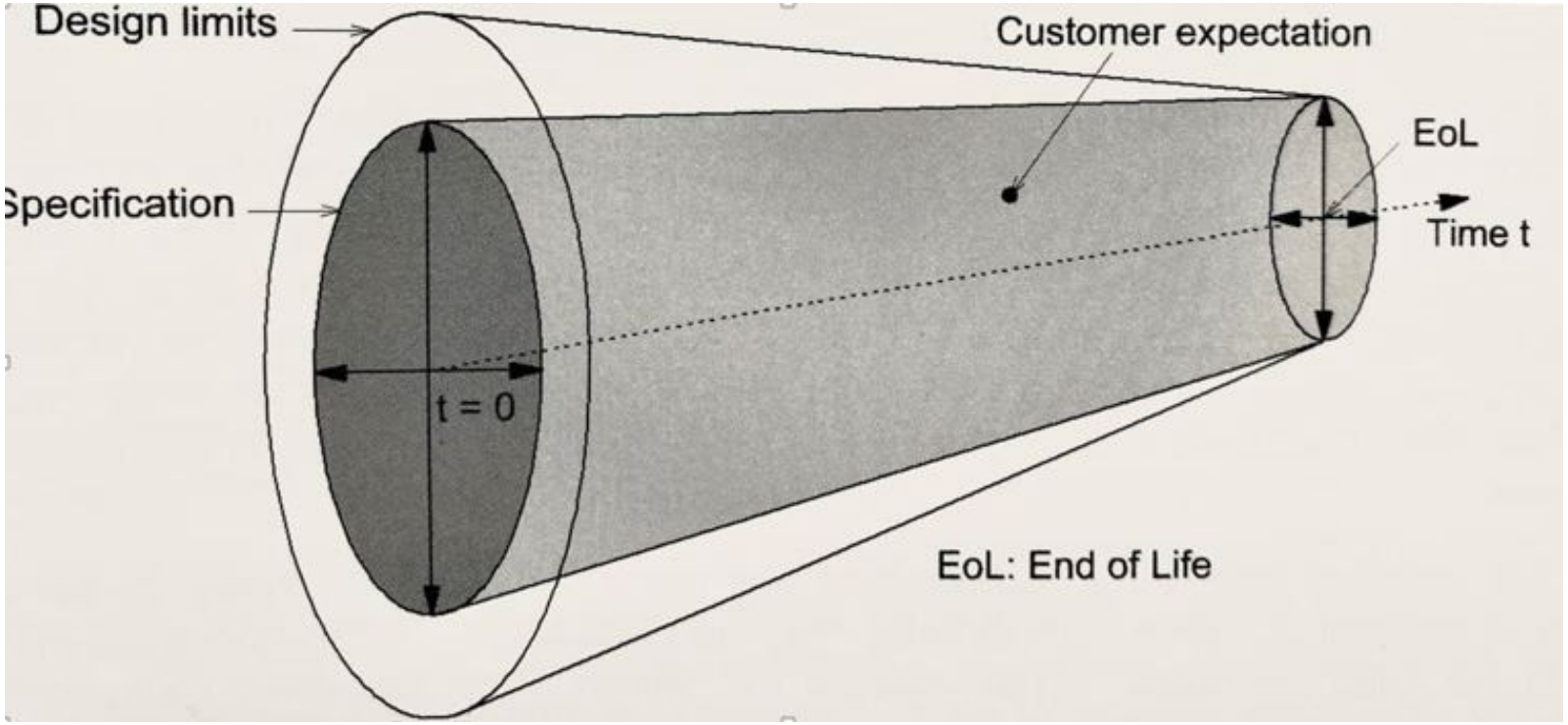


(a) (b)

TABLE II
TYPICAL LIFETIME TARGET IN DIFFERENT POWER ELECTRONIC APPLICATIONS

Applications	Typical design target of Lifetime
Aircraft	24 years (100,000 hours flight operation)
Automotive	15 years (10,000 operating hours, 300,000 km)
Industry motor drives	5-20 years (60,000 hours in at full load)
Railway	20-30 years (10 hours operation per day)
Wind turbines	20 years (24 hours operation per day)
Photovoltaic plants	5-30 years (12 hours per day)

Design for Reliability: Rimmen Model – Robust Design Process



- “Sudden Failure” (spontaneous, unpredictable): eg a cosmic ray
- “Drift Failures” (predictable, which develop slowly over the time: “fatigue”)

Design for reliability : statistical units and accelerated tests

FAILURE RATE λ

N. Of components — *Total number of defects* — *Working time in the field*

$$\lambda = \frac{n}{N \cdot \nabla t} \qquad (4.0.2)$$ *Failure Rate*

Failure In Time

$$1\,FIT = \frac{1}{10^9 h} \qquad (4.0.1)$$ *#times system fails in 1 h normalized to 10^9 jours*

Eg. n=4, on tot N=8000 devices (**sold** in the field!) on 5000h

$$\lambda = \frac{4}{8000 \cdot 5000h} = \frac{1}{10^7 h} \Rightarrow \lambda = \frac{10^{-7}h^{-1}}{10^{-9}h^{-1}} = 100\,FIT$$

Mean Time Between Failure

$$MTBF = \frac{1}{\sum \lambda} \qquad MTBF = \frac{1}{FIT} \qquad (4.0.5)$$

Sum over several components of the system (chips... wires)

the most defective components dominate the MTBF

$$ppm = \frac{n_{failed}}{n_{delivered}} \cdot 10^6$$ (Field returns, samples excluded)

RELIABILITY – DESIGN FOR RELIABILITY

Accelerated test law

$AF = \frac{t_{op}}{t_{Stress}}$ **Acceleration Factor** **Eq. 14.5**

Generally, a test can be accelerated if, for example, temperature, voltage, or the rates of change are increased.

Different acceleration models are used, depending on the focus of the test i.e. which failure mechanism is to be examined (Eq. 14.6 to Eq. 14.9). Common to all is that the operating test point (indexed as "stress") is set higher than the target operating point in the later application (indexed as "op"). The tests are performed on a selected number of components in order to validate the electrical, mechanical and thermal parameters as specified in the datasheet. Furthermore, these type tests also serve to determine the test limits of routine tests in the current production.

Arrhenius Model[1]	$AF(T) = e^{\left[\gamma\left(\frac{1}{T_{op}} - \frac{1}{T_{Stress}}\right)\right]}$	Eq. 14.6
Eyring Model	$AF(U,T) = AF(T) \cdot e^{\left[B\cdot(U_{Stress} - U_{op})\right]}$	Eq. 14.7
Peck Model[2]	$AF(RH,T) = AF(T) \cdot \left(\frac{RH_{Stress}}{RH_{op}}\right)^n$	Eq. 14.8
Coffin-Manson Model[3]	$AF(\Delta T) = \left(\frac{\Delta T_{Stress}}{\Delta T_{op}}\right)^c$	Eq. 14.9

Note: FIT depends by Application conditions temperature of usage and stats observations.

Eg SKIM4 2013-2021 → MTBF= $0,25 \cdot 10^8$, $T_{op} = 85°C$

Reliability Requirements and Reliability Tests

Reliability requirements

- Temperature and current density increasing
- Severe environmental conditions
- Extension of MTBF for critical applications (automotive…)

The needs of “accelerated tests”

- Failure criteria
- Test for **chip qualification** (HTRB, HTGS, H3TRB)
- Test for **Package Stability** (LTS, HTS, TC, PC)
- Test for **mechanical integrity** (V, MS)

Failure Criteria

	Name	Conditions	Standards
HTRB	High temperature reverse bias test[a]	MOS/IGBT: 1000 h, T_{vjmax}, V_{CEmax}(≤ 2.0 kV), 0.8 × V_{CEmax}(> 2.0 kV)	IEC60747-9:1998
		Conv: 1000 h, T_j = 125°C, V_{RM} = 0.9 × V_{RRM}, V_{RM}/V_{DM} = 0.8 × V_{RRM}/V_{DRM}[c]	IEC 60747-2/6 Kap. V
HTGS (HTGB)	High temperature gate stress test[a]	1000 h, ± V_{GEmax}, T_j = 125°C	IEC60747-9:1998
H3TRB (THB)	High humidity high temperature reverse bias test[a]	1000 h, 85°C, 85% RH, V_{CE} = 0.8 × V_{CEmax}; however, max. 80 V, V_{GE} = 0 V	IEC60749:1996
LTS	Low temperature storage test[b]	T = T_{stgmin}, 1000 h	IEC60068-2-1
HTS	High temperature storage test[b]	T = T_{stgmax}, 1000 h	IEC60068-2-2
TST	Thermal shock[a]	T_{stgmin} − T_{stgmax}; −40°C to +125°C, but ΔT_{max} ≤ 165 K $T_{storage}$ ≥ 1 h T_{change} ≤ 30 s High power, standard: 20 cycles High power, traction: 100 cycles Medium power: 50 cycles Conv.: 25 cycles[c]	IEC60749:1996

	Name	Conditions	Standards
TC	Temperature cycling[a]	External heating and cooling 2 min. < $t_{cycl.}$ < 6 min; ΔT_C = 80 K, T_{cmin} = 5°C High power, standard: 2000 cycles	IEC60747-9:1998
		Medium power: 5000 cycles Conv.: 5000 cycles[c]	IEC60747-2/6 Kap. IV
TC	Temperature cycling[b]	Two-chamber air system, T_{change} ≤ 30 s T_{stgmin} − T_{stgmax}: 100 cycles Conv. modules: 25 cycles[c]	IEC60068-2-14 Test Na
PC	Power cycling[a]	Internal heating and external cooling 0.5 < T_{cycl} < 10 s; ΔT_j = 60 K T_{jmax} = 125°C, 130,000 cycles	IEC60747-9:1998
PC	Power cycling[b]	Internal heating and external cooling ΔT_j = 100 K, 20,000 cycles Conv. modules: 10,000 cycles[c]	IEC60749-34
V	Vibration	Sinusoidal sweep: 5 g, 2 h per axis (x, y, z)	IEC60068-2-6 Test Fc
MS	Mechanical shock	Half-sine pulse, 30 g, three times	IEC60068-2-27 Test Ea

(a) Infineon, (b) SD

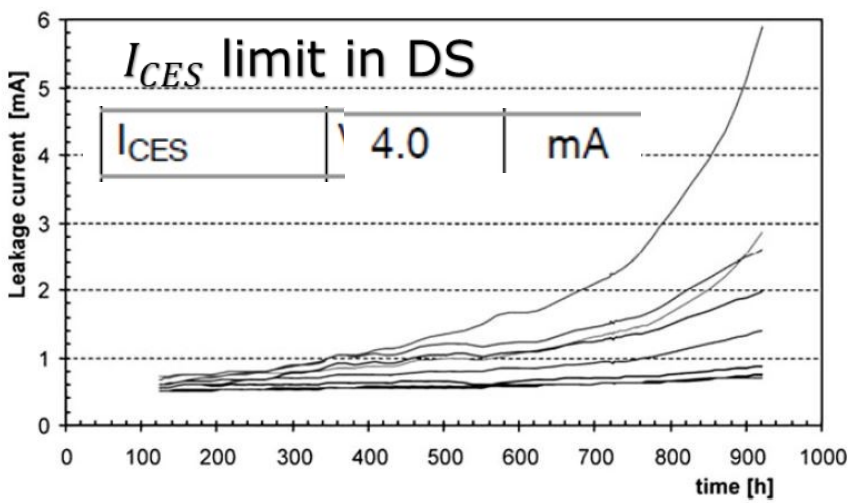
Failure criteria IEC60747-9(2001)	
I_{GSS}/I_{GES}	+ 100% USL
I_{DSS}/I_{CES}	+ 100% USL
$R_{DS(on)}/V_{CE(sat)}/V_F$	+ 20% IMV
$V_{GS(th)}/V_{GE(th)}$	+ 20% USL − 20% LSL
$R_{th(j\text{-}c)}/R_{th(j\text{-}s)}$	+ 20% IMV
V_{ISOL}	Not below specification limit

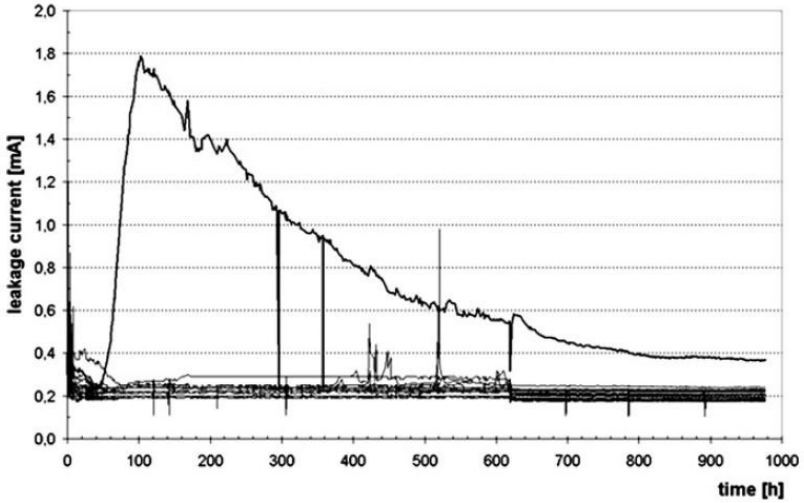
USL, upper specification limit; LSL, lower specification limit; IMV,

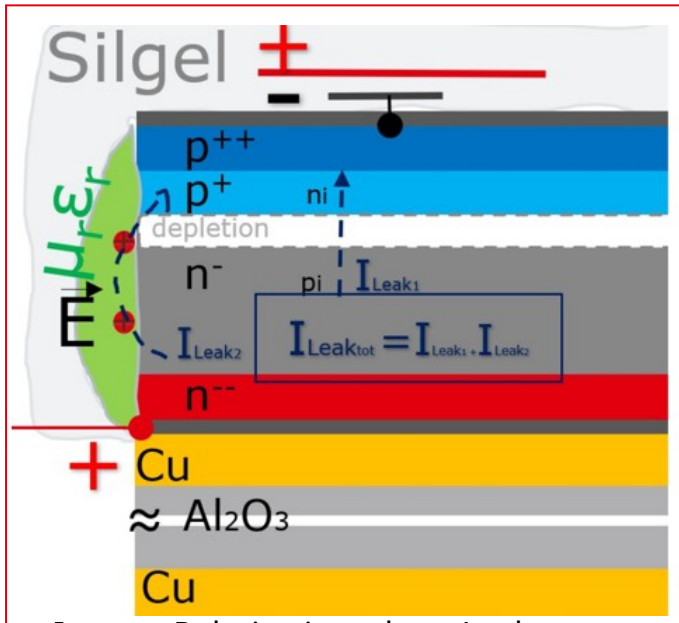
IMV : *Initial Measured Value*

Reliability Tests : HTRB (chip qualification)

- Tested in Inverse, and close to Tj,op
- Long term current losses stability
- Residual of the production process can impact this test
- Leakage current constant monitoring
- Examples of 8 DUTS and failure after 900 hours
- Residual and contamination could increase the accumulation of mobile ions which could cause passivation degradation of the junction and leakage increase.
- Possible to detect also tome design defect of the package







Inverse Polarization where Leakage comes from

Post test analysis highlighted missing of the “ring loop” of one chip wire bond . After bond wire layout correction the “peak” disappeared

Reliability Tests : HTGS (chip qualification)

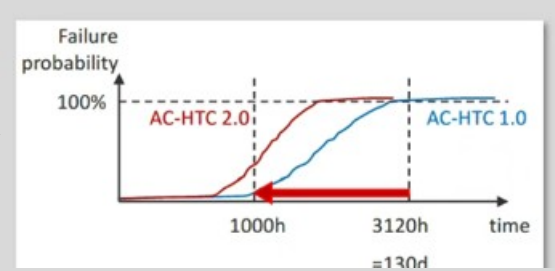
- Monitor the IGBT or MOS current gate current losses stability (max limited to ±20V)
- Thin dioxide surface of 100 nm generate intense Electric field through the gate oxide (2MV/cm! even at few volts like ±20V)
- Gate oxide must be defect free (*otherwise Tunnel Effect is facilitated*!)and only low surface carriers' density is acceptable
- Test is accelerated by increasing the max T_{jop}
- As the losses current trough the oxide are very small (< 10nA) the test is very sensible to eventual contaminations (*thermocouples+glue perturbation increase gate losses for instances*!)
- Possible cause of failure is production residuals (glue solvents… etc…)
- So this test is also important to verify the cleanliness of the chip surface during assembly

THB ($H3_{(V,T°C,Hum)}TRB$ or HV-H3TRB) (chip qualif)

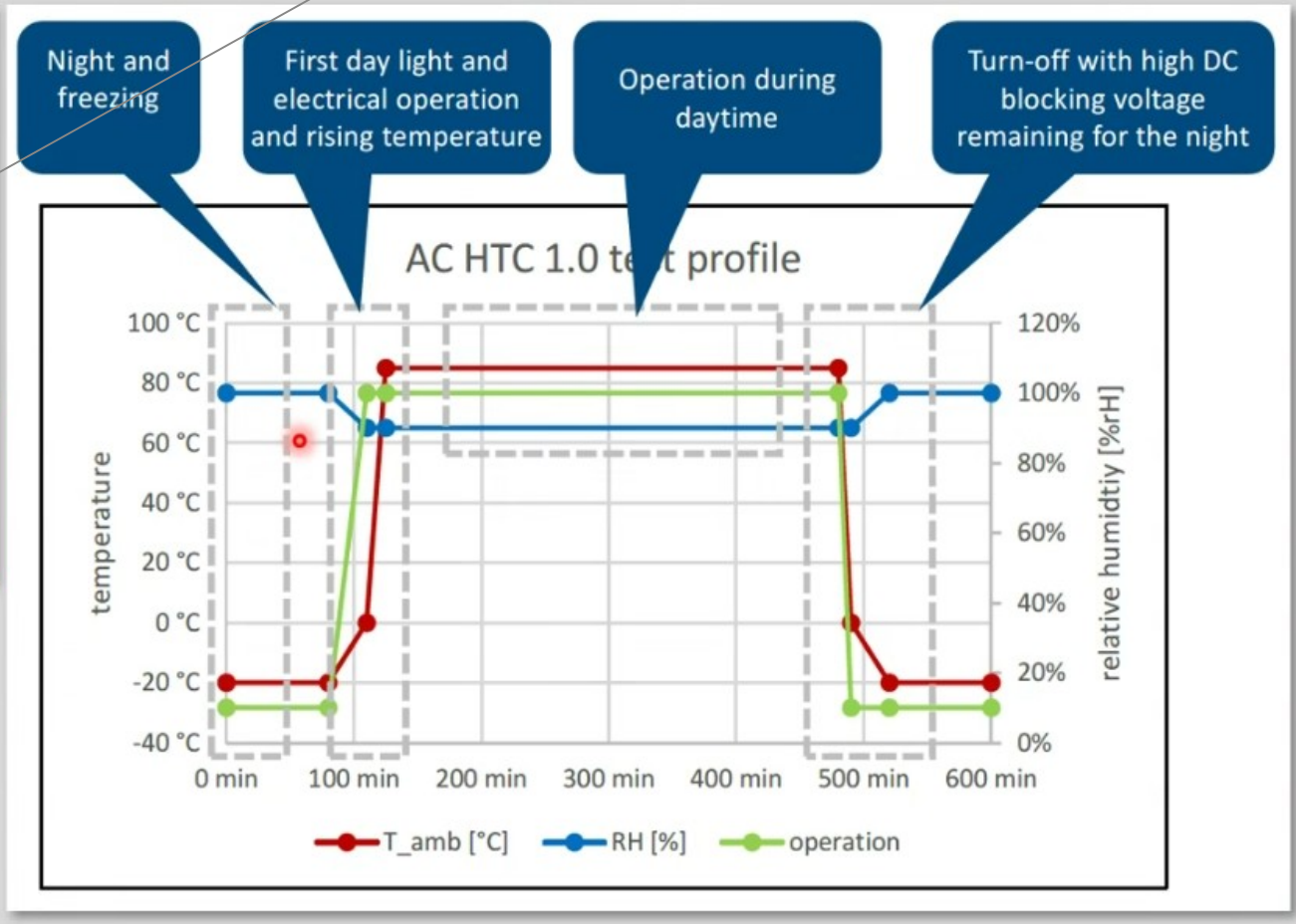
- This test evaluate the impact of the impact of the humidity on the long term performances.
- Perfect sealing is not possible (and even unwanted for the condensation creation or for high linear coefficient expansion of the silgel)
- Silgel/soft mould can be penetrated by water ions accelerated by high electrical field.
- The test target is to detect weak points of the chip passivation or process contaminations.
- The current target is 80% of maximum voltage limited to 80V but new chip technology allow to go beyond this limit (from H3TRB to HV-H3TRB which is mandatory requirement for Solar application for instances)
- Possible to enhance the stress of the HVH3TRB during switching conditions, the so-called “climatic test under operation” (*see after: for PV system need to simulate the night/day transient, and also static inverse operation is not realistic in real operations!*)
- *The impact of second soldering…*

AC-HTC

Alternating Current – Humidity Temperature Cycling



Test	Conditions	time	Comments
HTRB	T = Tvj,max; Vgs = 0V; Vds=80%...100% Vnom	1000h	No humidity
H3TRB	T = 85°C; rH=85% Vgs = 0V; Vds=80V	1000h	Very low voltage level
HVH3TRB	T = 85°C; rH=85% Vgs = 0V; Vds=80% Vnom	1000h	Harsher and more realistic requirements then H3TRB
AC-HTC	T = -20°C...85°C; rH=85...100%; Vds=66% Vnom Active operation	>3000h	Even more realistic to PV field scenario than HVH3TRB and reproducing specific field failures



background

- Findings in humidity robustness of early SiC devices in 2010
- Under standardization?

Reliability Tests : HTS LTS High/Low Temperature STORAGE (Package Qualification)

- Target is to verify plastic materials integrity over life time.
- To be intended as **NON operative temperature** limit for assembled Power Module (it is NOT a storage limit of not-assembled modules…)
- Soft mould can have degradation at temperatures higher than 180°C.
- Low temperature is critical for plastic materials and they lose elastic capabilities.
- The same the silicon soft gel “cracks” at temperatures below -55°C.
- Non operative storage limits for power modules are typically -40°C / +125°C.
- New application require this range to be extended: this will generate more challenges for this test in future.

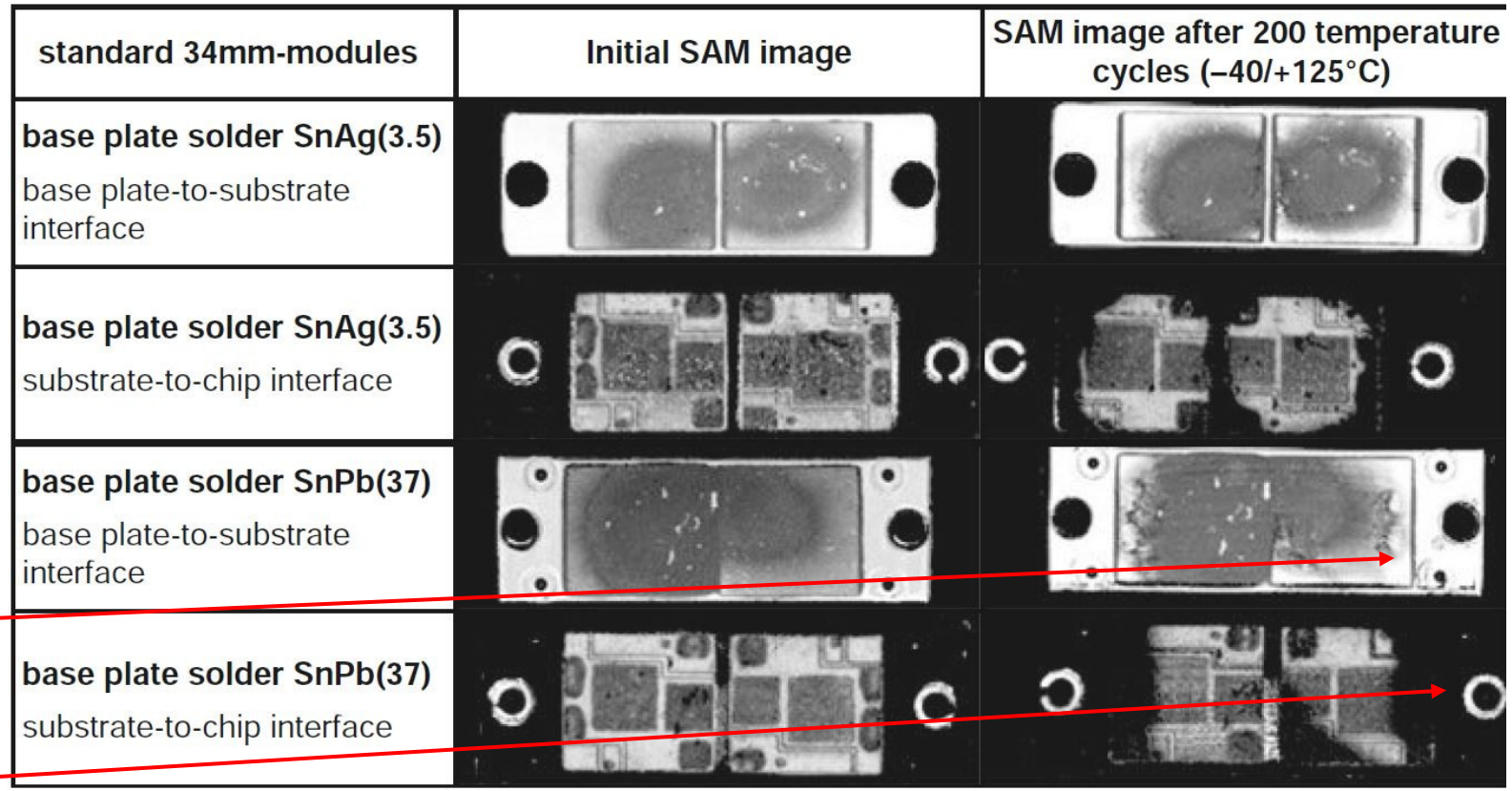
Reliability Tests : TC and TS (1/2) (Package qualification)

- Temperature Cycling → temperature (from *EXTERNAL* sources) change rate between 10°C and 40°C in one minute. No Voltage (the temperature is changed by external sources)
- Temperature Shock → Temperature changes in rate below than 1 min (air chamber with elevator, or if faster with liquid to liquid : warm oil and liquid nitrogen: not for power modules, YES for DBCs)
- Need to reach the temperature equilibrium after the change (between 30 minutes and 2 hours)
- The definition “temperature cycling” can be slightly different from different power module manufacturers
- The test simulate the temperature change from external sources → the DUT is not under operation!

Reliability Tests : TC and TS (2/2)

This test cause mechanical stress on materials with different thermal expansion coefficients and the effect can be evaluated by delamination or cracks on the copper/Al2O3 layers with SAM analysis

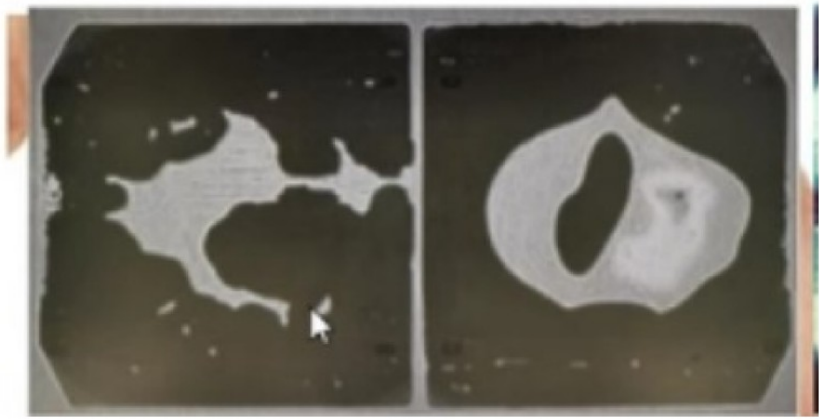
Here two solder materials are evaluated on module with 34mm baseplate. Standard SnPb(37) after 200 thermal cycles from -40°C to 125°C performed with two air chamber show more “white” areas (high acoustic reflexion) due delamination which absorbs the acoustic wave). Black areas indicate absence of acoustic reflection because delamination(*)



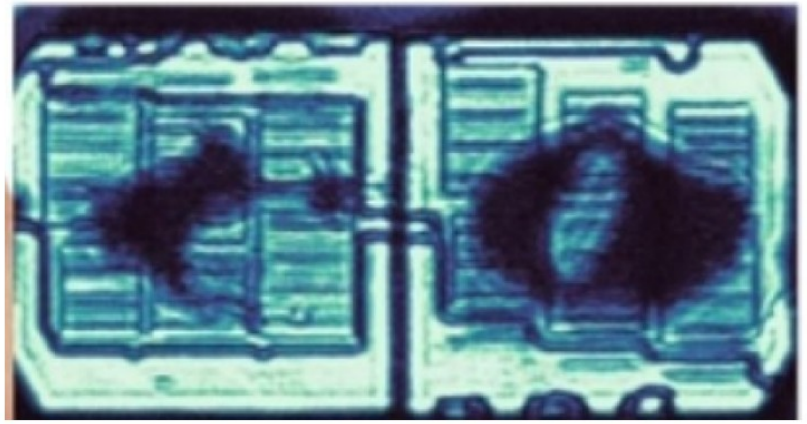
(*) SAM signal it sent from baseplate surface , closer reflections reduce the power signal which does not penetrate the deeper layer

Conventional SAM vs Laser (Optical) Microphone based SAM

- Conventional SAM has better resolution vs X-Ray for detecting voids between baseplate and DCBs
- Conventional SAM need mechanical parts and the microphone to interface acoustic signals received by reflection and transformation to electrical signals to be analyzed in post-processing.
- New technologies(1) make usages of laser microphones (or optical microphones): based on principle that *sounds impact speed of light!*
- Photo-Acoustic imaging: Fabry-Perot Interferometer. Acoustic pressure modify the air refraction index. This change the optical wave-length of the light transmission. **No mechanical parts needed → faster**
- Much better resolution and sensibility of X-Ray (good for in-line mass production test) but still not able to detect small cracks (so for post-processing analysis after thermal cycling reliability test still conventional SAM is better)



Solder voids detected by C-SAM



Solder voids detected by laser microphone

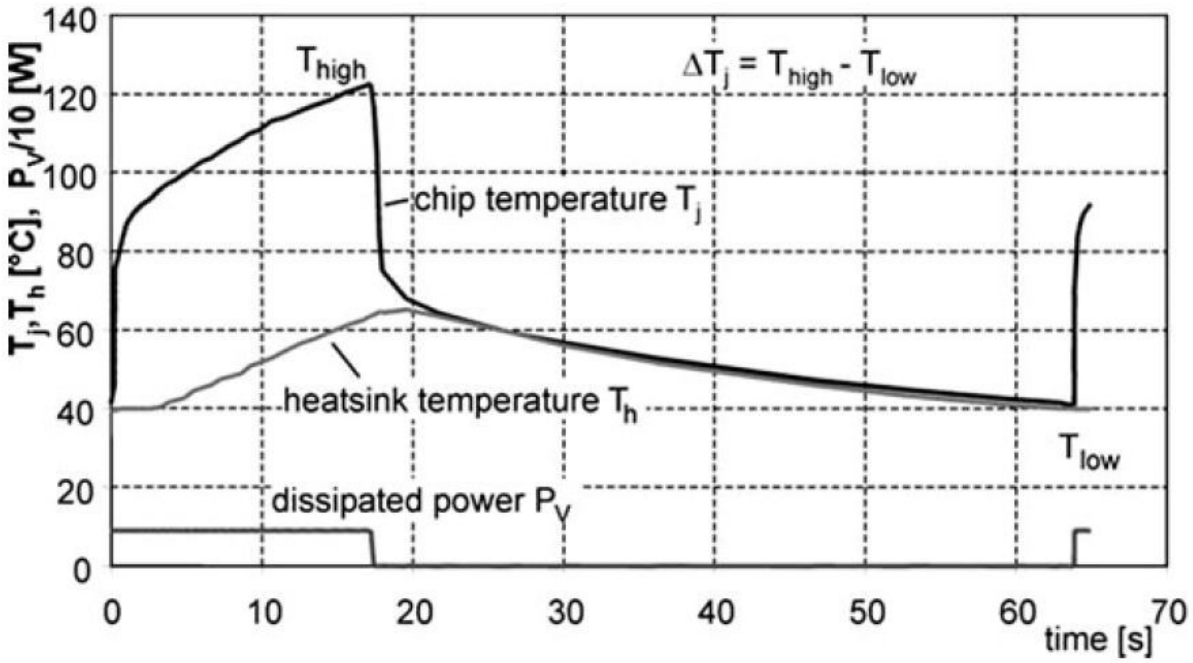
(1) XARION, https://xarion.com/en/technology/technology

Balthsar Fischer, *Optical microphone hears ultrasounds,* Nature Photonics, June 2016, Vol 10 N.6

Preißer S., Fischer B. and Panzer N. , *Listening to Ultrasound with a Laser,* Optik & Photonik Volume12, Issue5, Dec 2017

Package Stability: Reliability Tests : PC (1/4)

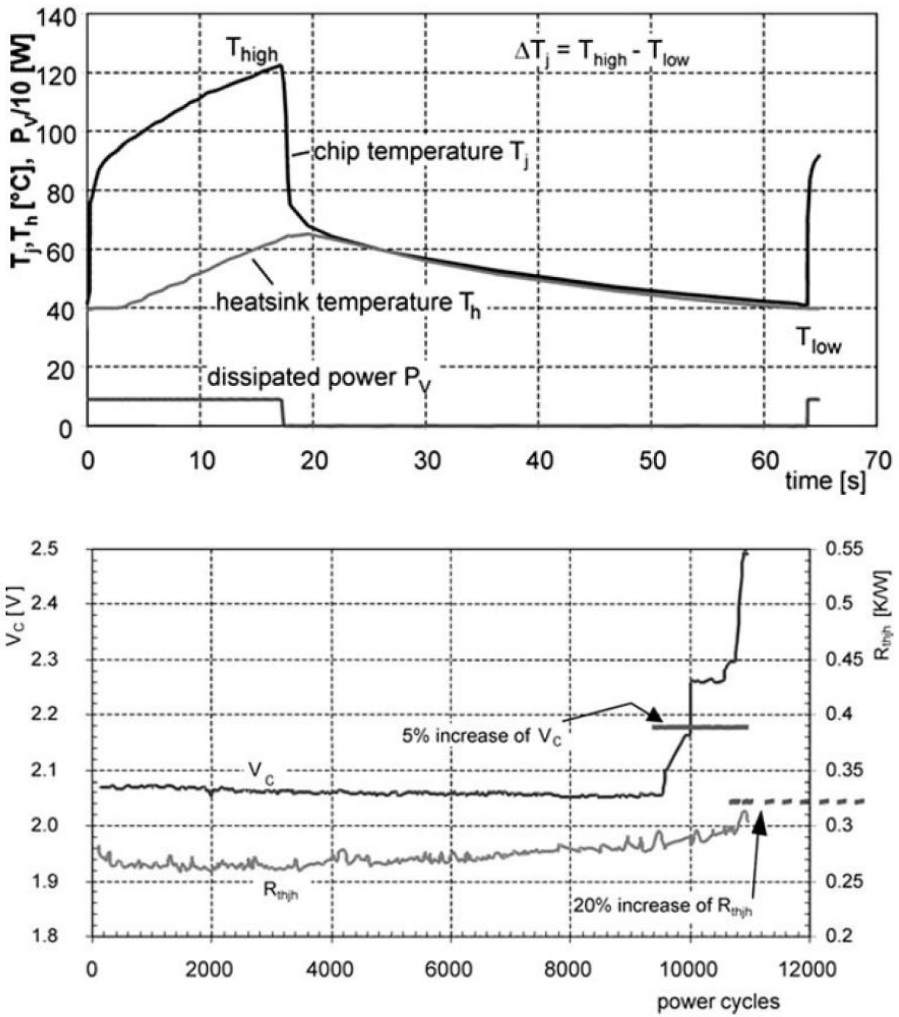
- Power Cycling is performed with active chip which warm the module with the electric dissipation during cyclic switch on and switch off
- This test target the chip power losses mounted on a specific modules, so it is key to qualify the chip itself **working on a specific package**.
- The smaller is the chip the more challenge is this test as power dissipation is more critical
- DUT is mounted on heatsink under nominal working condition. After reaching of $T_{vj,max}$ the DUT is switch off and cool down is started
- When T_{min} is reached the current is switch on again and the cycle restart.
- A significant temperature gradient is generated during the test



Example of Power Cycling test and temperature shape during the cycling

Reliability Tests : PC (2/4)

- Heatsink temperature is used for control purpose.
- Typical PC parameter is $\nabla T_j = T_{high} - T_{low}$ n the picture
- Another key parameter is $T_m = T_{low} + \frac{T_{high} - T_{low}}{2}$
- Longer temperature cycle represents higher stress
- This thermal stress leads to the generation of *fatigue* marks on materials which can he highlighted by the increase of forward Voltage which is constantly monitored
- Thermal resistance ($R_{th\text{-}jh}$ initial value is *measured* with the
- Rth NOT steady state $R_{th(a-b)} = \frac{T_a - T_b}{P_V} = \frac{\nabla T}{P_V}$
- R_{thjh} increasing during the test cause also an increase of the V_C which is typical indication of the reached limit of PC (in this case after 90k cycles)

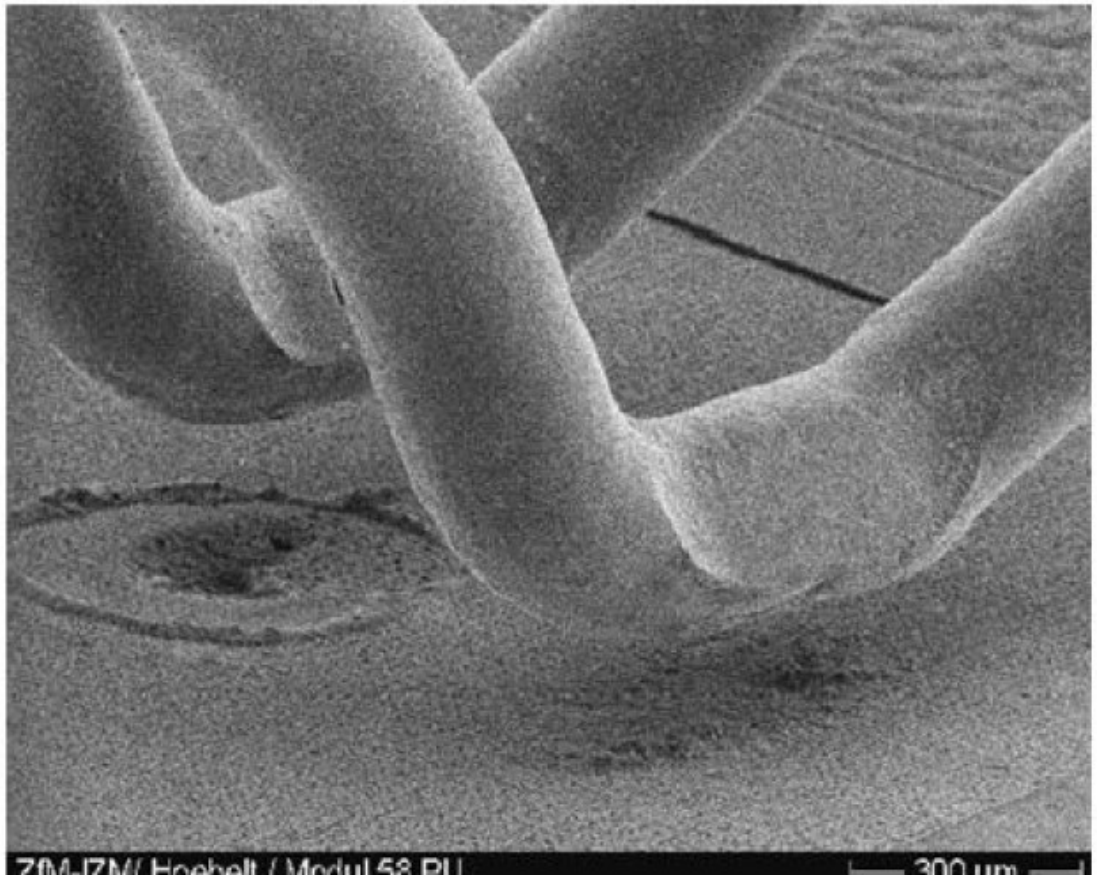


Reliability Tests : PC (3/4)

- A first 5% VC increase can be an indication of bond wire lift off.
- This cause further increase of the resistance and further static losses till the bond wire damaging
- This cause the reaching of EOL

Failure conditions for the PC tests

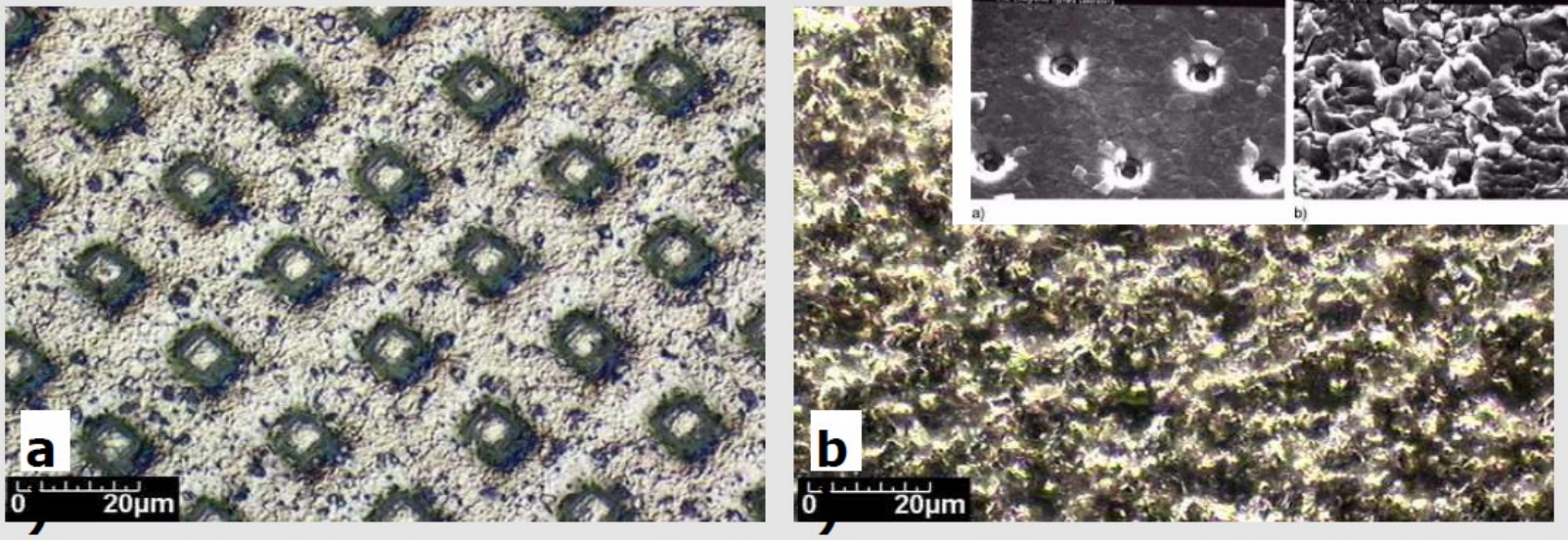
- VC increase from 5% to 20% depending by measure accuracy. First step is due to bond wire lift off.
- R_{th} increase beyond the 20% values “measured” at the starting of the test (this is NOT the Rth indicated in DS which is STEADY STATE! But for comparison purpose is ok to use this measure)
- Failure of typical device characteristics (f.i blocking capability or gate emitter isolation capacity



Reliability Tests : PC (4/4)

Bottle-neck during power cycling is often the wire-bond. But especially for “small” chips this could not be the case and also the chip surface can generate failure mechanism

Recostruction of Al chip surface (Power Cycling)



a) Microscopic image of emitter metallization of chip from phase not cycled (cell structure clearly visible)

b) Microscopic image of emitter metallization of failed chip after power cycling test (cell structure not visible)

Failure mechanism of power cycling
→ Destruction of chip metallization

Reliability test limits depend by the application!

Motor drive: 100Kcycles (elevator OTIS!)

UPS, Solar : 15kpcs is ok!

PC and TC stress require CTE similar for different materials.

SiC life times is 1/3 of IGBT (Ok for Solar and UPS where efficiency is the key parameter. Not OK where PC 100Kcycles is required)

Design strategy to increase the PC/ TC level

- Removing Baseplate
- Sinter technology

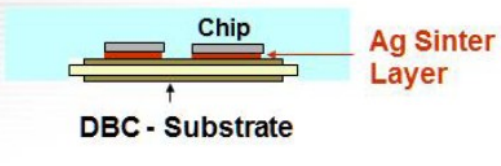
Stress!

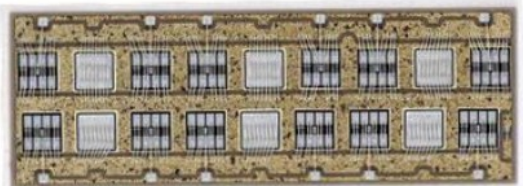
Example: Length L = 1cm; dT=100K

Material	CTE 10^{-6}/K	T [°C]	ΔT [K]	ΔI Power Cycling	T [°C]	ΔT [K]	ΔI Temperature Cycling
Chip (IGBT) Si	3,5	125	100	3.5µm	125	100	3.5µm
AlN -DCB	8,2	105	80	6.6µm	125	100	8.2µm
Al_2O_3 - DCB	10,7	105	80	8.6µm	125	100	10.7µm
AlSiC base plate	7	80	55	3.8µm	125	100	7µm
Cu base plate	17	80	55	9.4µm	125	100	17µm
Bond wire Al	23	100	75	17.2µm	125	100	23µm

Figure 2.7.9 Linear expansion of different material layers in a power semiconductor module with an assumed edge length of 1 cm. Left: for a temperature gradient in the module as for a typical power cycle; right: for heating up the entire module as for temperature cycling with identical ΔT

Sinter-Technology: removing of chip solder joint





material	CTE 10^{-6}/K	T [°C]	dT [K]	dL Temperature Cycling
die (IGBT)	4	125	100	4.1µm
Ceramic AlN	4,4	125	100	4.7µm
Ceramic Al_2O_3	8,3	125	100	8.3µm
~~Baseplate~~	~~17~~	~~125~~	~~100~~	~~17µm~~
Bond wire* Al	23	125	100	23µm*

Stress does not disappear, but sinter layer is able to handle the stress!

Reliability: Challenges for the Future

H2S requirements

HALT test

Mission Profile

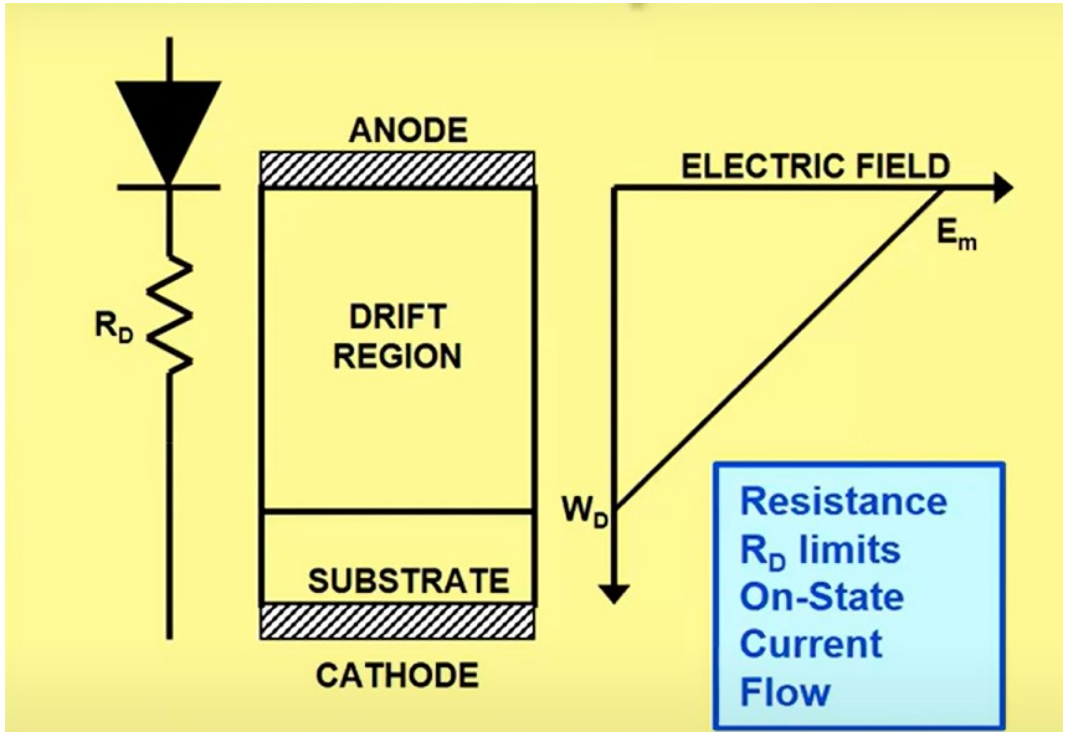
Challenges for the Future

- Current density continuously increase and silicon area decreasing
- Power density
- PC test for wideband gap material (SiC, GaN)…
- Switching frequency increase ad Stray Inductance limits
- Efficient way to drain heating
- HVH3TRB more than 2000 hours, H2S …

Power Electronics

8: Emerging applications in power electronics based on Silicon Carbide and Gallium Nitride

Wide Band Semicondutcors Power Devices



$$R_{ON,SP} = \frac{4BV^2}{\varepsilon_S \mu_n E_G^3} \Rightarrow \frac{4BV^2}{\varepsilon_S \mu_n E_C^3}$$

Baliga's Figure of Merit (BFOM) for Power Semiconductor Devices:

$$BFOM = \varepsilon_S \mu_n E_C^3 = \frac{4BV^2}{R_{ON,SP}}$$

Goal: Low On-State Power Loss

Rif: , **J. Balyga** *My Quest for the Ideal Power Switch*, NC State ECE Lecture 09/2023

https://www.youtube.com/watch?v=mDnOyzMpu1s&t=22s

Overview

Strong covalent bonds between Si and C make SiC extremely hard, chemically inert and with high thermal conductivity

It has wider “forbidden” band gap , so more difficult to bring electron from the valence band to the free electron state (conduction band) and is more difficult to have “impact” ionization

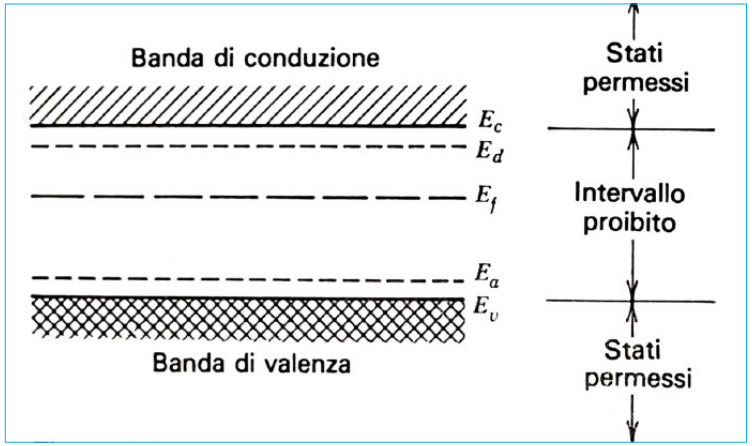
Silicon T_{jmax}=150°C. After $T>T_{jmax}$ n_i inside *p-type* (or p_i inside *n-type*) start becoming preponderant and p-n junction inverse polarized loses his isolating characteristics

[Ec-Ev](SiC)>>[Ec-Ev](Si) → Tjmax SiC 200°C theoretically up to 1000°C.

Corollary→ SiC easy to develop cooling system (smaller)

Note: Power Cycling bottle neck often due to “surrounding” materials not to SiC! (less bond wires as SiC chips smaller, plastic, CTE…

“Baliga Figure of Merits” linked to the semiconductor properties



$$n_i^2 = N_c N_v \exp\left(\frac{-E_g}{kT}\right)$$

$$R_{ON} = \frac{4V_{BD}^2}{\varepsilon_s \mu_n E_C^3}$$

$$\text{BFOM} = \epsilon_s \mu_n E_C^3$$

Figure of Merit (BFOM) comparison SiC vs Si and R_{ON}

Hexagonal, 4 bistrateRamsdell notation

SiC R_{ON}<< Si R_{ON} because the material characteristics

$$R_{ON} = \frac{4V_{BD}^2}{\varepsilon_s \mu_n E_C^3}$$

Critic BrD El

	Si	GaAs	4H-SiC	GaN
BFOM $=\epsilon_s \mu_n E_C^3$ (normalized to Si)	1	17	119	537
Bandgap (eV)	1.11	1.43	3.26	3.5
Breakdown Electric Field (V/cm)	$3 \cdot 10^5$	$3.5 \cdot 10^5$	$35 \cdot 10^5$	$35 \cdot 10^5$
Electron mobility μ_n (cm^2/Vs) at $300K$	1350	6000	800	1200
Relative dielectric constant ϵ_s	11.8	12.8	9.7	9

SiC enable much higher performances than Silicon

SiC MOS usually can have higher Voltage BD level (reason why Si MOS does not exist at 1200V and at parity of voltage shows much higher R_{ON})

R_{ON} key DS characteristics

V_{DS}	1200 V
I_D @ 25°C	63 A
$R_{DS(on)}$	32 mΩ

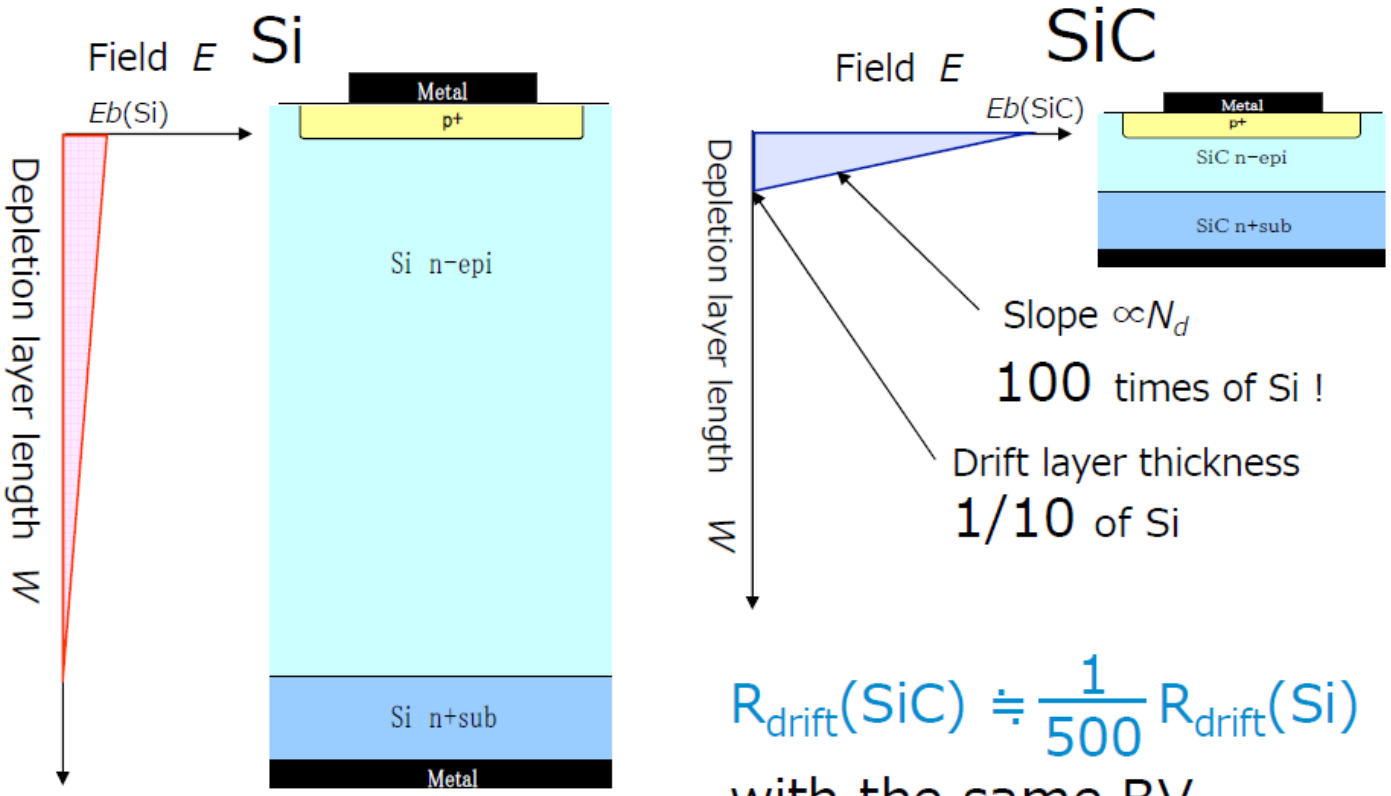
Silicon Carbide Power MOSFET
C3M™ MOSFET Technology

CREE

Comparison MOS Unipolar SI vs MOS Unipolar SiC (not in scale)

In off-state, high voltage is blocked with
n- epi layer (drift layer)
⇒In on-state, drift layer is current path => Ron

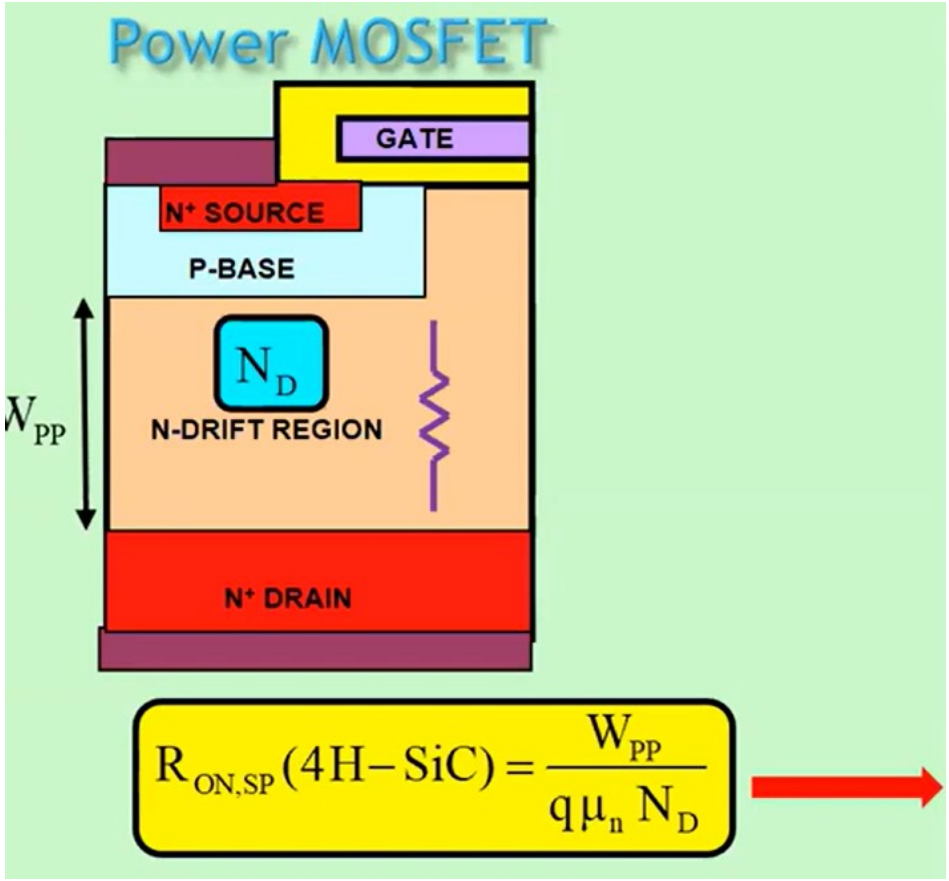
Blocking voltage is equivalent to the area of triangle => $V_b = E_b W/2$



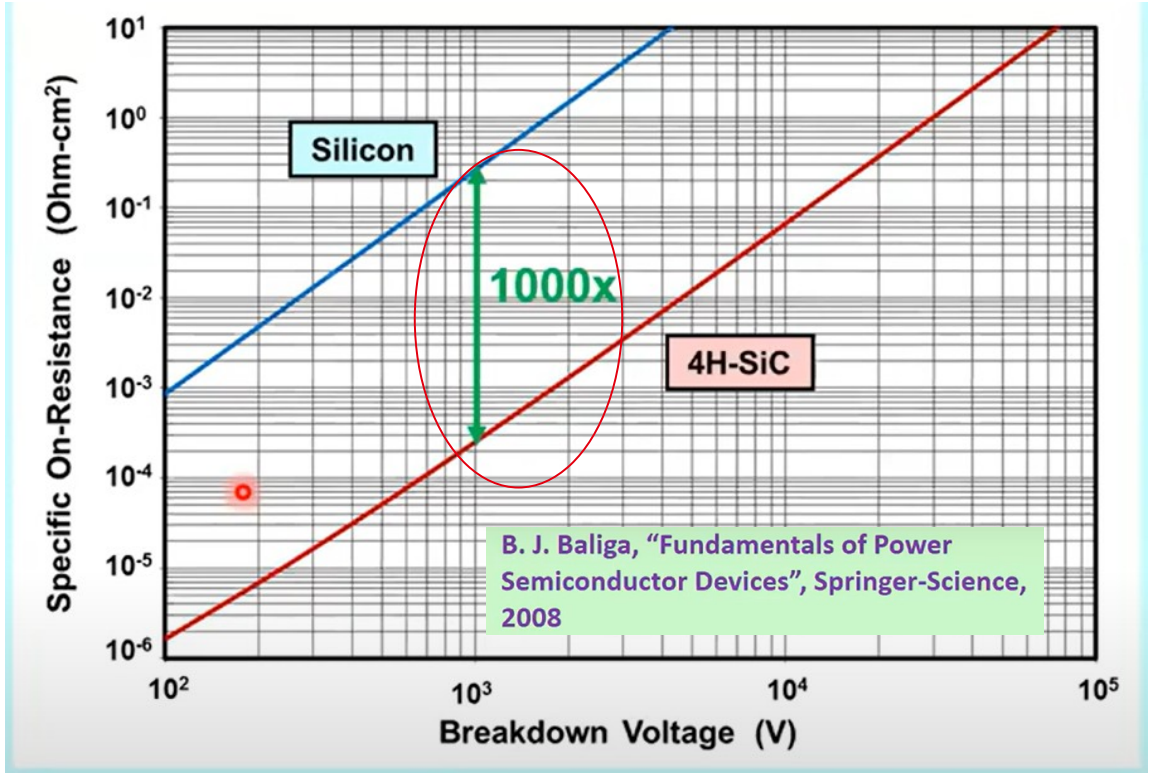
$$R_{drift}(SiC) \doteqdot \frac{1}{500} R_{drift}(Si)$$

with the same BV.

Power SiC MOSFET : R_{ds_ON} vs Silicon



$$R_{ON,SP}(4H-SiC) = \frac{W_{PP}}{q\mu_n N_D}$$



$$W_{PP}(4H-SiC) = 2.33 \times 10^{-7}\, BV^{7/6}$$
$$N_D(4H-SiC) = 1.98 \times 10^{20}\, BV^{-4/3}$$
$$\mu_n(4H-SiC) = \frac{4.05x10^{13} + 20N_D^{0.61}}{3.55x10^{10} + N_D^{0.61}}$$

Market Tends

TRANSFORM: Trusted European SiC Value Chain for a Greener Economy

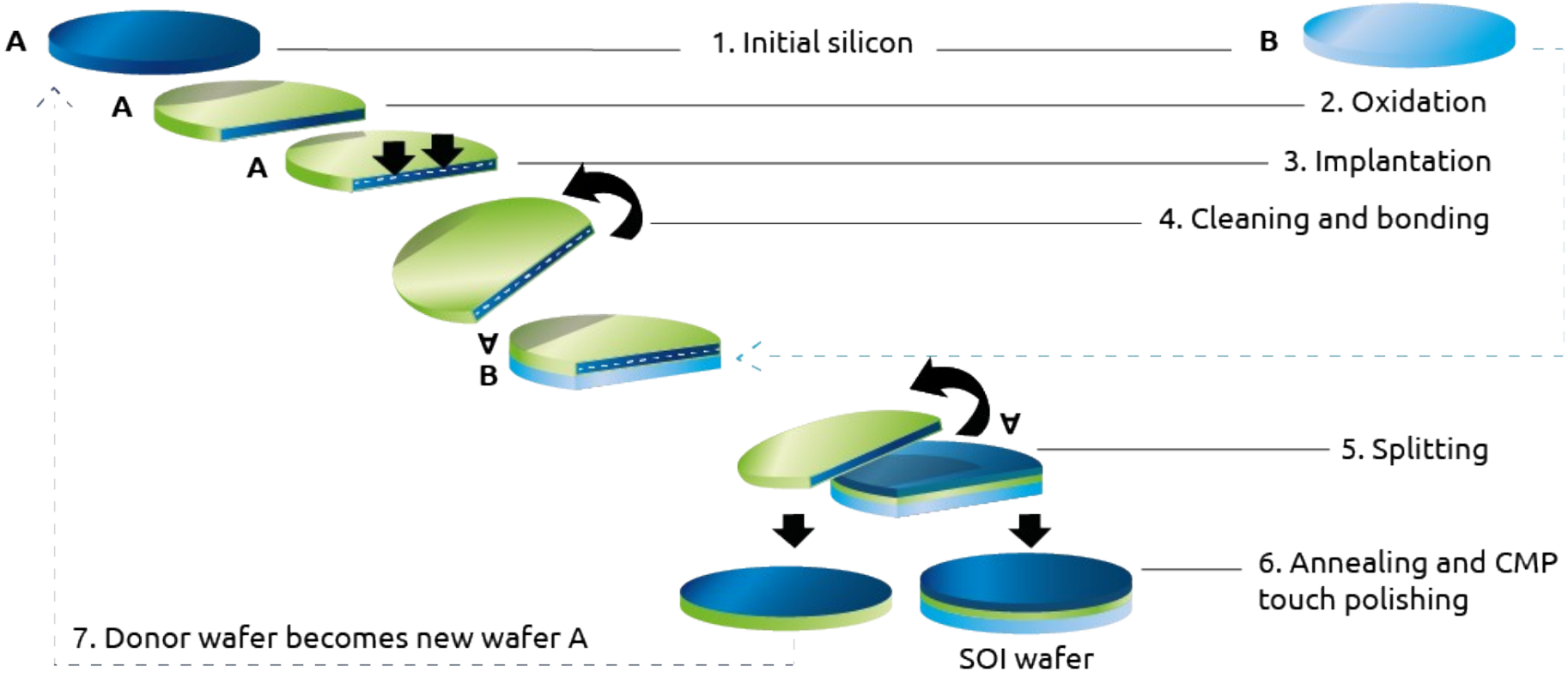
Complete EU supply chain from silicon wafer to system demonstrators

Supply chain critical (pandemy, geopolitical situation) but also EU SiC gap vs US/Japan

New factory 8 inches SiC STM started

Advanced SiC Manufacturing Technology

- SiC with conventional manufacturing of single crystal ingots: 2400°C (vs 1500°C for Si)
- Time: several weeks for growth (vs some days for growing time in Si)
- Smart-Cut idea: growth single crystal wafer on poly-silicon wafers and re-usage



Application landscape

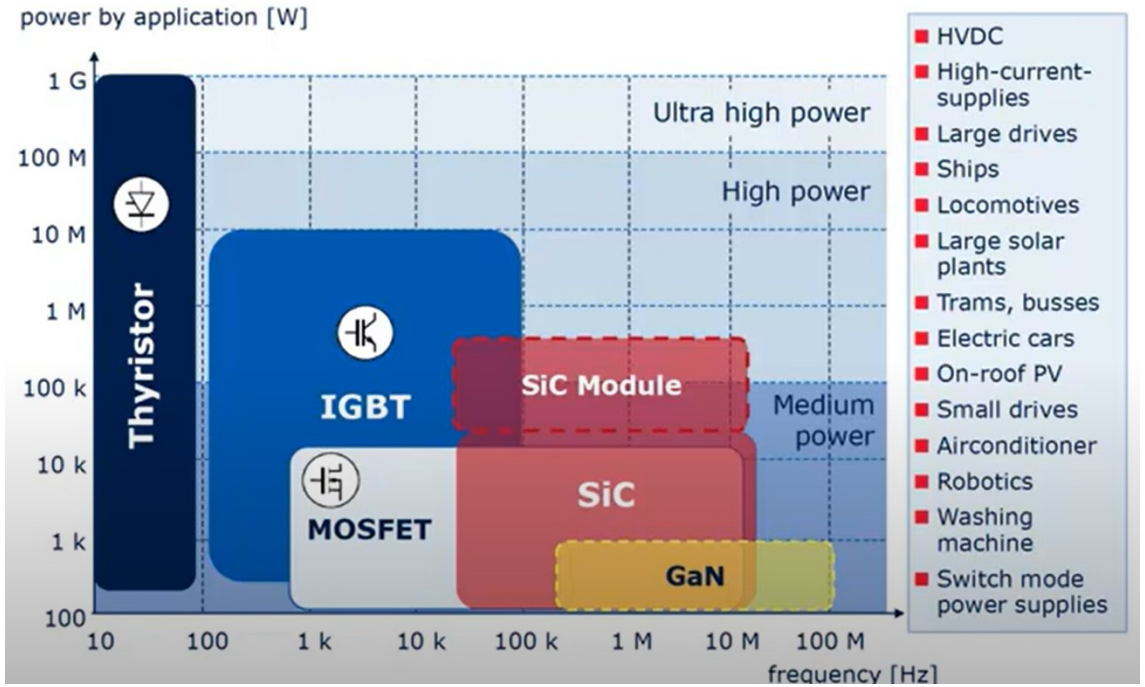
SiC and GaN not new! Already known

- GaN : High frequency , RF , satellites where €/A is never a problem (Power Electronics → commodities → cost is a bigger KPI). GaN : widely used in optoelectronics Laser Blue (Blue Ray!)
- SiC much more used and studied in Power Electronics but also in space → wider gap → less sensibility to Cosmic Ray , impact ionization (CAL4 is silicon and is less sensible too→ exploit but is an exception)

Still cost gap vs Silicon of 1 order of magnitude

2011 forecast (source IFX) on Power vs Frequency application (will expand more in area typically served by silicon (lower frequency and higher power) the more cost optimization will happen

IFX 2011



Esempi di convertitori DC-DC “leggeri”, “ottimizzati nei costi” e ad “alta efficienza” per automotive

Product Portfolio
Power Modules

Shower Power® Technology

Bond Buffer® Technology

DCM™

Flexible Design through Customization
Si IGBT and full silicon carbide MOSFET technology
750V/1200V half-bridge design for up to 900 A_{rms}
DBB Sintering Technology for high reliability
Low thermal resistance thanks to ShowerPower®3D
Robust molded module packaging, low warpage and reliable mechanical integration
Highest power density
Multisourcing thanks to chip independency

Direct Pressed Die Technology®

eMPack®

High Performance Package for e-mobility
Silicon carbide MOSFET and full silicon carbide technology
750V / 1200V Sixpack compatible package for up to 900A_{RMS}
Double Sided Sintering package for automotive grade reliability
Low thermal resistance thanks to DPD Technology
Flexible cooler arrangements
2.5nH package stray inductance including terminals
Multisourcing thanks to chip independency

Peak power of Vicor´s automotive product line modules:
BCM6135-A06 800V to 48V and 48V to 800V – unregulated 2.5 kW
DCM3735-AN2 48V to 12V and 12V to 48V – regulated 2.0 kW and
PRM3735S-AB4 48V to 48V – regulated 2.5 kW.

- Vantaggi chiave
  - Riduzione della massa e del peso e quindi del costo (nelle applicazioni automotive è un aspetto chiave)
  - Miglioramento efficienza, riduzione dei consumi

- Fonti:
- Bodo’s Power #Novembre 2024
- Semikron Danfoss

Riferimenti per la fisica quantistica e dei semiconduttori

[1] *Introduzione alla fisica dei Quanti*, Giovanni Battimelli, Seminario tenuto al liceo Classico Mamiani di Roma il 20/03/2014. disponibili su YouTube `https://youtu.be/ky-55xzuTeQ?si=m26p2yl3VZKOuGPQ`

[2] *Fisica Matematica Logica,* Valerio Pattaro - (link consultato il 09/11/2024) ,`https://www.youtube.com/@ValerioPattaro`

[3] C. Mencuccini, V. Silvestrini, *Fisica II Elettronagnetismo - Ottica*, Liguori Editore, Terza edizione Italiana: 1998

[4] C. Mencuccini, V. Silvestrini, *Fisica I Meccanica Termodinamica* , Liguori Editore, Seconda edizione Italiana: 1987

[5] Mazzoldi P., Nigro M., Voci C., *Fisica, Eletromagnetismo e Onde*, EdiSES, Terza Ddizione Italiana: 2021

[6] R.P. Feynman, R.B. Leighton, M. Sands, *La Fisica di Feymann , volume 3 Meccanica Quantistica,* Zanichelli seconda edizione 2007.

[7] J. Milman, A. Gravel, *Microelettronica*, McGraw-Hill, 1994 (edizione italiana)

[8] R. Muller, T. Kamis, *Dispositivi Elettronici nei Circuiti Integrati*, Bollati Boringhieri, 1993

[9] G. Vaccaro, A. Carfagna, L. Piccolella, *Lezioni di geometria e algebra lineare* - Zanichelli 1999

[10] Papoulis, A. *Probability, Random Variables, and Stochastic Processes* - Third International Edition - McGraw Hill 19991

[11] Iannaccone, Giuseppe, Corso di Elettronica di Potenza, Università di Pisa. A.A. 2012-2020, disponibili su YouTube

[12] N. Mohan, T.M. Undeland, W. P. Robbins, *Power Electronics, Converters, Applications and Design*, Third Edition, John wiley & Sons, Inc, 2003

[13] Neil W. Ashcroft, N. David Mermin *Solid State Physics* - Harcourt inc. 1976. Versione consultata in francese: *Physique des solides,* EDP Science, 2002.

[14] Luigi Palumbo, Le Origini della Teoria Quantistica, *Appunti del corso di Fisica Moderna 2017-2018, Lezione 4,* disponibile on line all'indirizzo https://www.sbai.uniroma1.it/sites/default/files/LEZIONE%20N.4%20-%20CONDUZIONE%20NEI%20SOLIDI.pdf

[15] Sze S.M.,Kwok K.NG. *Physics of Semiconductor Devices,* 2007, John Wiley & Sons, Inc.

[16] Sze Simon M. *Dispositivi a Semiconduttore Comportamento fisico e Tecnologia*, Hoepli 1991.

[17] Ledermann Leon, Hill Christopher T. *Fisica quantistica per poeti,* 2013, Bollati Boringhieri (ed. or. 2011 *Quantum Physics for Poets*)

[18] Peter W. Atkins, *Chimica Fisica, terza edizione condotta sulla quinta edizione inglese,* Zanichelli, 1997

[19] *Classic Papers in Physics*, Hans Kangro editor, 1972

[20] Segré Emilio, *Personaggi e scoperte della fisica contemporanea,* Mondadori 1996

[21] Segré Emilio, *Personaggi e scoperte della fisica classica,* Mondadori 1996.

[22] Fleisch D. *Guida allo studio dell'equazione di Schrodinger,* Editori Riuniti 2021

[23] Pierret F. Robert, *Advanced Semiconductor (vol VI) Fundamentals, 2nd edition,* Prentice Hall 2003

https://nanohub.org/courses/sfun (Mark Lundstrom, Perdue University, ultimo accesso al link : 16/03/2025)

Riferimenti per la parte di elettronica di potenza

[1] Iannaccone, Giuseppe, Corso di Elettronica di Potenza, Università di Pisa. A.A. 2012-2020, disponibili su YouTube

[2] A. Volke, M. Hornkamp, *IGBT Modules Technologies, driver and applications*, Infineon Technologies AG, Third edition , 2017

[3] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, *Application Manual Power Semiconductors*, SEMIKRON International GmbH, 2nd revised edition 2015

[4] J. Lutz, H. Schlangenotto, U. Scheuermann, R. De Doncker, *Semiconductor Power Devices Physics, Characteristics, Reliability,* Springer, 2011

[5] N. Mohan, T.M. Undeland, W. P. Robbins, *Power Electronics, Converters, Applications and Design*, Third Edition, John wiley & Sons, Inc, 2003

[6] J. P. Uyemura, *Fundamentals of MOS Digital Integrated Circuits*, Addison-Wesley Publishing Cpmpany, 1998

[7] SEMISEL, *SEMIKRON Power Electronic Simulation Tool*, `https://www.semikron-danfoss.com/service-support/semisel-simulation.html,SEMIKRON-DANFOSS`

[8] PSIM 2021A, *Simulation environment for power conversion and motor control*, `https://powersimtech.com/products/psim/capabilities-applications, POWERSIM`

[9] N. H. E. Weste, K. Eshragan, *Principle of CMOS VLSI Design*, 2nd edition 1993

[10] C. Mencuccini, V. Silvestrini, *Fisica II Elettronagnetismo - Ottica*, Liguori Editore, 1998

[11] J. Milman, A. Gravel, *Microelettronica*, McGraw-Hill, 1994 (edizione italiana)

[12] M. Santoro, M. Hansmann, M. Muscolino, *SEMiX5 Technical Explanations, Revision 03, 23-06-2021* `https://www.semikron-danfoss.com/dl/service-support/downloads/download/semikron-technical-explanation-semixr5-en-2021-06-23-rev-03.pdf`

[13] `https://youtu.be/bmsWgA8bxdA`

[14] T. Kioto, J.A. Cooper, *Fundamentals of Silicon Carbide Technology*, John Wiley & Sons, IEEE PRESS, 2014

[15] R. Muller, T. Kamis, *Dispositivi Elettronici nei Circuiti Integrati*, Bollati Boringhieri, 1993

[16] B. Jayant Baliga, *The IGBT Device Physics, Design and Applications of the Insulated Gate Bipolar Transistor,* Elsevier, 2015

[17] B.J. Baliga, *Semiconductors for high voltage vertical channel field effect transistors,* J. Appl. Phys. 53 (1982) 1759-1764

[18] `https://www.soitec.com/en/products/smart-cut`

[19] P. Beckedahl, J. Rudzki, M. Spang, *Trends in Power Module Packaging and Impact of Wide Bandgap Semiconductors*, SEMIKRON-DANFOSS, ETG 2023

Riferimenti “classici” per i dispositivi e moduli di potenza (IGBT, MOS,…)

Matteo Santoro
Commissione Elettronica e Microelettronica Ordine degli Ingegneri della provincia di Roma
matteos72@gmail.com

Product Manager Semikron Danfoss
matteo.santoro@semikron-danfoss.com

Mobile: +39 333 1285194